Operator's Manual

30-263289

**MODEL 8828D AND MM8103A,
MM8104, MM8105, MM8106
WAVEFORM DIGITIZING SYSTEM**

OFFICIAL RECORDS
FILE
FACILITIES

LeCroy

Innovators in Instrumentation

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GENERAL INFORMATION

Using This Manual

This manual provides installation and operation instructions for the 8828D Waveform Digitizing System. It's organized such that technical density builds through ensuing sections. Your knowledge of modular waveform digitizing systems should determine where you begin.

INSTALLATION

SECTION 1 introduces the 8828D in its working environment. This "System" approach adds perspective for the First-time User who could benefit from a detailed Product Description. For users with little or no programming experience, we propose our optionally available WAVEFORM CATALYST Software as the turnkey solution to your digitizing needs.

ASYST Programmers can take advantage of LeCroy's 6920-DL Digitizer Driver Library Package option. The LeCroy drivers are fully integrated with the ASYST language format. They employ English-like command words to make all GPIB and CAMAC commands totally transparent to the user. SECTION 1 also covers module configuration and installation, adding memory, and cable attachments.

OPERATION

SECTION 2 contains operating instructions for programming the 8828D module using either LeCroy's 8901A or 6010 GPIB to CAMAC interface (controller). Separate sections address WAVEFORM-CATALYST Users, ASYST Programmers, and GPIB<=>CAMAC Programmers. SECTION 2 also includes special sections on BURST Mode, BURST Generators, and Model 4222 BURST Generation.

THEORY OF OPERATION

SECTION 3 contains functional descriptions of the 8828D and its associated memory modules, and respective block diagrams. In addition, it contains comprehensive 8828D specifications.

Unpacking and Inspection

LeCroy recommends that the shipment be thoroughly inspected immediately upon delivery. All material in the container(s) should be checked against the enclosed Packing List and shortages promptly reported to the carrier. If the shipment is damaged, please notify the carrier immediately. If the damage is due to mishandling during shipment, you must file a damage claim with the carrier. Your regional LeCroy field service office can assist with this. LeCroy 100% tests all products before shipping. LeCroy ships all products in packaging designed to protect against reasonable shock and vibration.

Always identify an instrument's specific version by the Engineering Change Number (ECN) on its back panel.

Warranty

LeCroy warrants its instruments to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranties only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Factory or an authorized service facility within the warranty period, only if the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations. All replaced parts and products become the property of LeCroy Corporation.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

For all LeCroy products in need of calibration or service *after the warranty period*, the customer must provide a Purchase Order Number. The customer will be billed for parts, labor, and shipping.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy Corporation shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

Product Assistance

LeCroy Corporation will gladly answer your questions. Call your regional field service office, or ATS Sales and Service Division, 700 Chestnut Ridge Road, Chestnut Ridge, New York 10977-6499, (914) 578-6038.

Maintenance Agreements

LeCroy offers a selection of customer support services to meet your individual needs. Extended warranty maintenance agreements allow you to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, calibration, on-site repair, and engineering improvements are available through specific Supplemental Support Agreements. Please contact your regional field service office.

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Documentation Updates

LeCroy continually improves the performance of its products. Addenda may appear in this manual's back sleeve along with any errata.

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CAUTIONS

COOLING

The high power dissipation of the 8828D requires that it be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature to less than 50° C. To ensure optimal component cooling, install modules over cooling fans. See "Installation in Mainframe," (p 1-15) for preferred slot information.

TERMINATION RESISTORS

Proper installation of the memory modules requires removal of resistor terminators from all memories except the one furthest from the 8828D (see p 1-17).

BATTERY

Unsolder one lead of the battery or remove jumper E1-E2 before attempting repairs on these modules.

INSTALLATION

Turn off mainframe (crate) power during insertion or removal of module to avoid possible damage caused by momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

SECTION 1: INSTALLATION

8828D Waveform Digitizing System Overview

The LeCroy 8828D Waveform Digitizer provides the basic system core for high speed, long record waveform recording. The system modularity allows multiple channels, memory expansion, and mixing with other accessory modules or slower speed digitizers, thus providing flexibility for use in both large and small system applications.

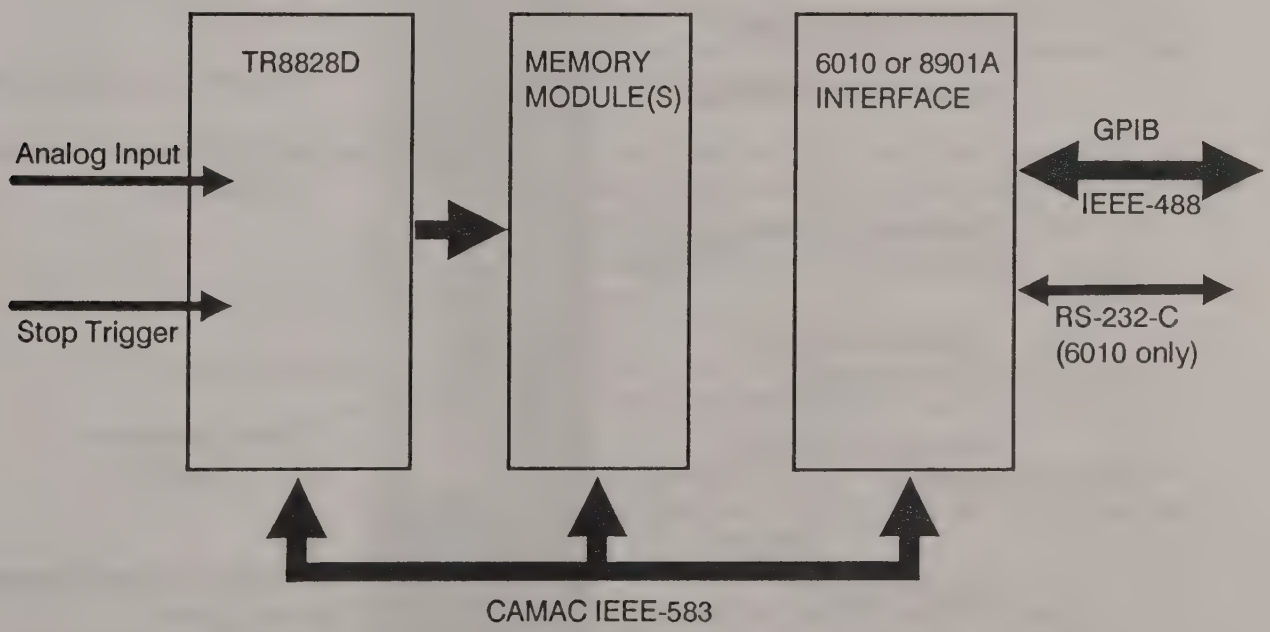


Figure 1: SYSTEM ARCHITECTURE

8828D WAVEFORM DIGITIZER

The 8828D Waveform Digitizer is optimized for digitizing and recording high frequency signals. This is evidenced by its wide bandwidth, fast sampling rate, and dynamic accuracy (i.e., effective bits) even for signal frequencies approaching the Nyquist limit. Even the minimum system (32 ksamples) offers large memory capability. Long memory stores high frequency signal detail by allowing digitization over long periods. Moreover, the memory is easily expandable when it is necessary to record extremely long records.

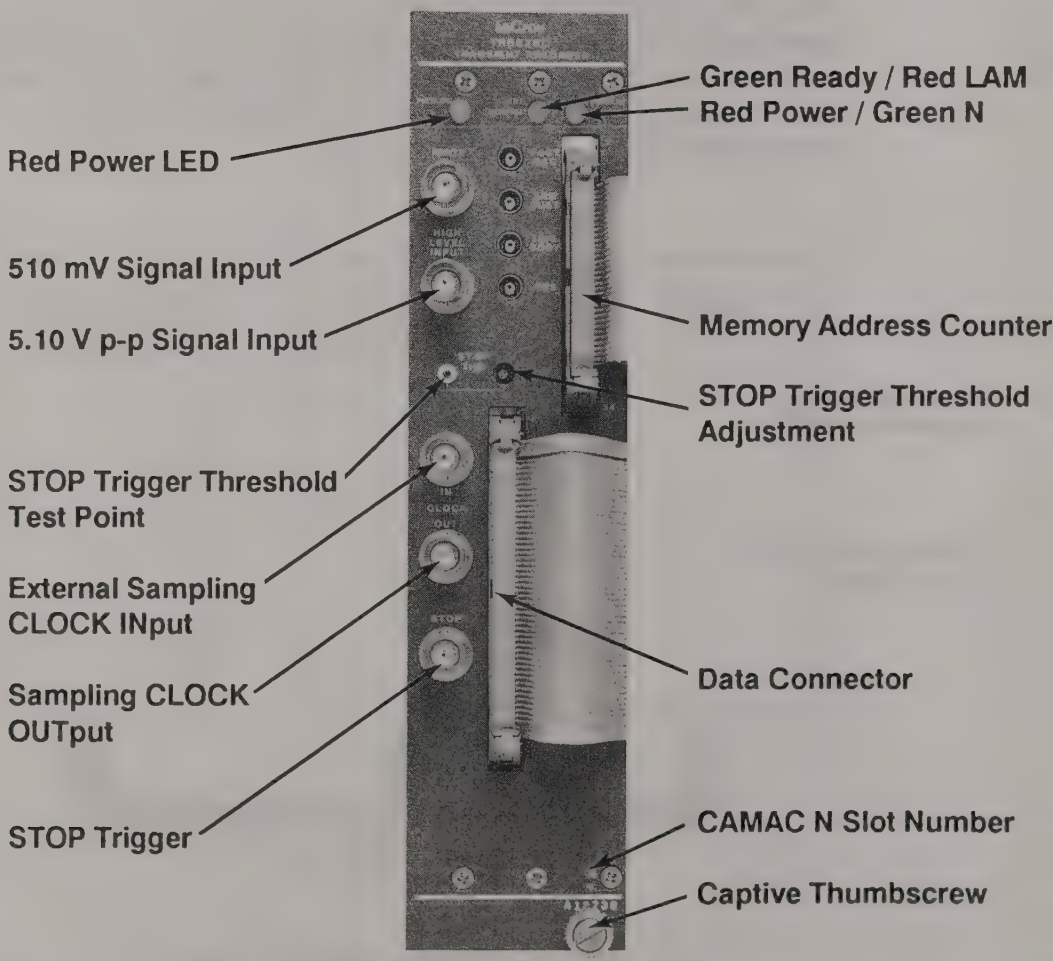


Figure 2: 8828D Waveform Digitizer

FEATURES

LeCroy's 8828D Waveform Digitizer features:

High Digitizing Rate	Maximum sampling rate of 200 MS/sec (5 nsec between points)
Wide Analog Bandwidths	The analog bandwidth of >100 MHz provides the ability to record high frequency signals while maintaining high signal fidelity.
Exceptional Accuracy	8-bit resolution and low distortion provide high dynamic accuracy to preserve signal characteristics over the entire frequency range.
Large, Expandable Memory	From 32K to 2M sample points permit capturing signals with poorly correlated triggers, and allow the recording of fine detail on signals of long duration. Special configurations offer up to 640 M sample memory.
Memory Retention	Contents of data memory and control registers are internally battery backed-up for up to 1 year.
External Clock	Permits operation with a clock from another digitizer or an external source. Clock rate can be any frequency from DC to 200 MHz.
Multiple Pulse	In BURST Mode, the memory accepts data only when enabled and can be used to store large numbers of closely spaced pulses by not recording the deadtime.
User Defined Trigger Controls	Adjustable slope and threshold level provide versatile triggering over ±2 V range.
Versatile Pretrigger	Up to 100% of the memory may be allocated to prerecording the waveform prior to the occurrence of the trigger.

Synchronization Outputs	Front-panel ARM BUSY and TRIG BUSY signals facilitate system coordination, and may be used to trigger other devices.
Programmable	Digitizers, and memory plug-ins may be externally controlled via GPIB or RS-232-C for automatic setup or unattended operation.
Compact	Suitable for benchtop operation or in configurations with up to 5 channels per rackmount chassis (LeCroy Model 1434A and 8025 mainframes).

MEMORY MODULES

LeCroy offers four different memory modules for storing waveform data during practical 8828D applications.

MM8103A The MM8013A provides 32 ksamples of memory per module at 100 MHz digital bandwidth. It must be used in pairs (a maximum 16 modules for 512 ksamples).

MM8104 The MM8104 provides 32 ksamples of memory at 200 MHz digital bandwidth. Only one MM8104 can be used with each 8828D.

MM8105 The MM8105 provides 128 ksamples of memory per module at 100 MHz digital bandwidth. It must be used in pairs (a maximum 16 modules for 2 Msamples).

MM8106 The MM8106 provides 512 ksamples of memory per module at 100MHz digital bandwidth. It must be used in pairs (a maximum 4 modules for 2 Msamples).

CAUTION: *Different memory module types cannot be mixed. Each 8828D can feed a memory system consisting of only one type memory modules.*

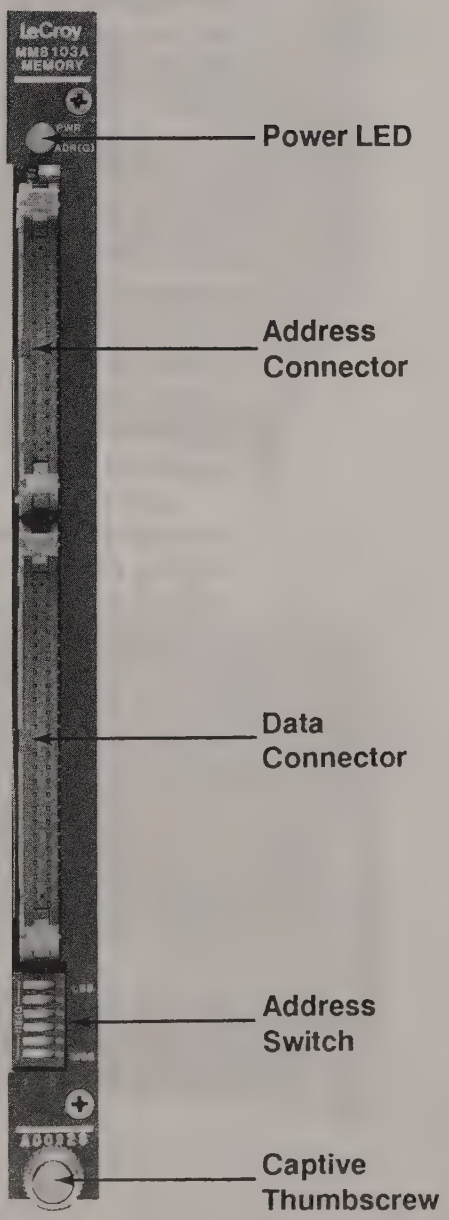


Figure 3: LeCroy Memory Module Connectors

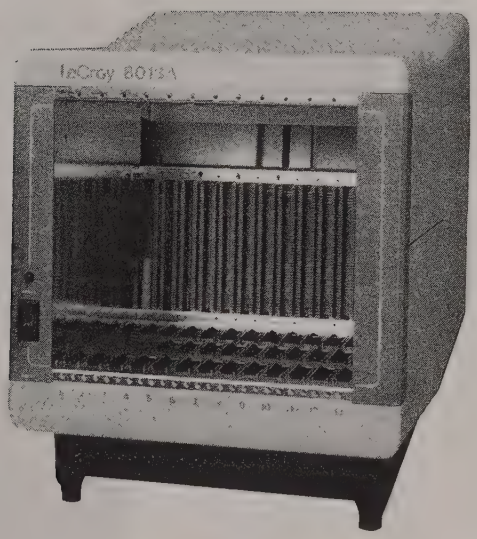
CENTURY SERIES System Configuration

The Model 8828D Waveform Digitizer can be purchased in a 1 or 2-channel CENTURY SERIES System. The CENTURY SERIES 2102 System includes 1 8828D/MM8104, the CENTURY SERIES 2002 includes 2 8828D's/MM8104's. Along with the 8828D(s)/MM8104(s) the CENTURY Systems include an 8013A benchtop mainframe, an IEEE-488 Standard GPIB to CAMAC interface, a GPIB cable and PC-based WAVEFORM-CATALYST Oscilloscope software. Or the 8828D module itself can be added into an existing CENTURY SERIES System for expansion.

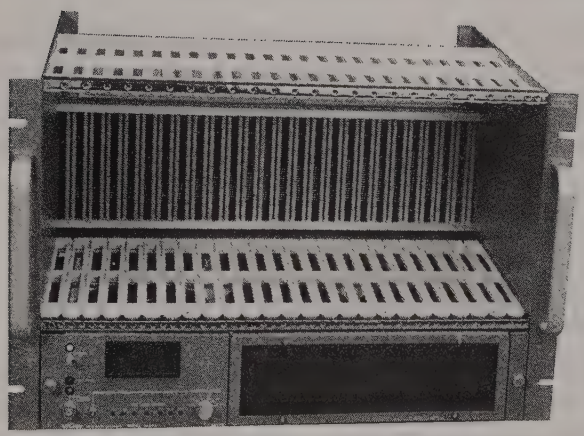
IEEE-583 Standard (CAMAC) Instrument Mainframes

LeCroy Benchtop Model 8013A, and Rackmount Models 1434A, and 8025 meet all requirements of the CAMAC Standard (IEEE-583), assuring unrestricted choice of modules from LeCroy or second-source CAMAC suppliers. They house the 8828D, its associated memory modules, and other LeCroy plug-in instrument modules. The 8013A benchtop accepts instruments in combinations of up to 11 single-width plug-ins when using a 2 slot controller module. The 1434A and 8025 rackmount series accommodate up to 23 instrument modules when using a 2 slot controller. Both single and multi-width plug-ins can be accommodated.

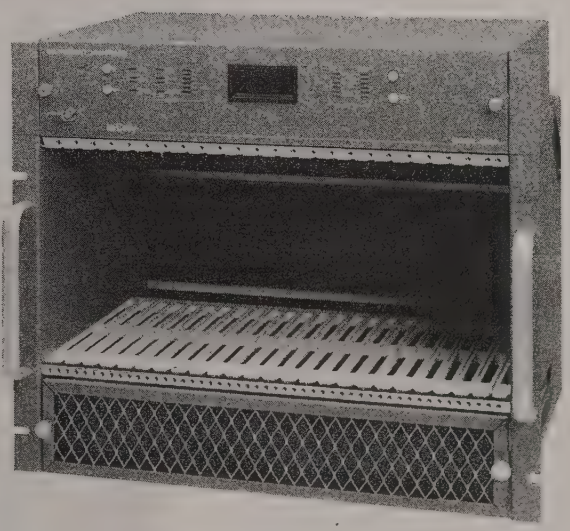
Versatility, user customization, and expandability are the prime advantages of LeCroy CAMAC based systems. Many more functions than could be practically or economically combined in a single instrument are available by selecting the appropriate LeCroy instrument and accessory modules.



8013A



1434A



8025

Figure 4: LeCroy Instrument Mainframes

Programming Environments

WAVEFORM-CATALYST Software

WAVEFORM-CATALYST Software converts an IBM PC/XT/AT, PS/2, or Compaq III/386 (or 100% compatible) and LeCroy digitizers into multi-channel waveform data acquisition systems. The software controls, acquires, displays, averages, histograms, saves/recalls, to/from disk, and prints waveforms.

ASYST Scientific Software

ASYST Scientific Software converts an IBM PC/XT/AT, PS/2, or Compaq III/386 (or 100% compatible) and LeCroy digitizers into waveform analyzers. Analysis includes +, –, /, x, area under curve, differentiation, filtering, FFT, IFFT, correlation, pulse parameters, curve fitting, interpolation, etc.

GPIB/CAMAC Programmed Operation

8828D CAMAC bus commands allow programmed GPIB control for automated test applications. GPIB programming is possible via LeCroy's 8901A or 6010 IEEE-488 (GPIB) to IEEE-583 (CAMAC) Interface controllers.

IEEE-488 (GPIB) to IEEE-583 (CAMAC) Interface

The 8828D Waveform Digitizing System employs either the 8901A or 6010 IEEE-488 (GPIB) to IEEE-583 (CAMAC) Interface (controller). Most 8828D functions are programmable (see Figure 8 for side-panel hardware configured features; trigger level is front panel adjusted). The GPIB to CAMAC interface provides bidirectional communication. A host computer can download control and setup commands to the 8828D and upload waveforms from the 8828D. The 8901A interface uploads at up to 450 ksample/sec; the 6010 at up to 600 ksample/sec.

8901A GPIB to CAMAC Interface

The 8901A converts a CAMAC mainframe with up to 23 individual instruments into a standard GPIB Talker/Listener. The 8901A is compatible with the user's host, whether it be a mainframe computer, dedicated instrument controller, or personal computer. Its block transfer mode allows transfer of all data from a CAMAC module upon receipt of a single talk command at rates up to 450 kilobytes/sec. continuously. The 8901A is fully compatible with both LeCroy's Series 6900 WAVEFORM-CATALYST Software and ASYST Scientific Software. Thus, remote control, data transfer, and simple program instruction of LeCroy instrument modules can be achieved via a personal computer.

Figure 5: 8901A Interface Module

6010 Manual and GPIB to CAMAC Interface

The 6010 MAGIC Controller converts a CAMAC mainframe with up to 23 individua instruments into a standard GPIB Talker/Listener. The 6010 is compatible with the user's host, whether it be a mainframe computer, dedicated instrument controller, personal computer, or RS-232-C serial terminal. Data transfer over GPIB is available in hex ASCII, decimal ASCII, binary, or floating point at rates up to 200 kilobytes/sec. The 6010 is fully compatible with both LeCroy's Series 6900 WAVEFORM-CATALYST Software and ASYST Scientific Software. Thus, remote control, data transfer, and simple program instruction of LeCroy instrument modules can be achieved via a personal computer.

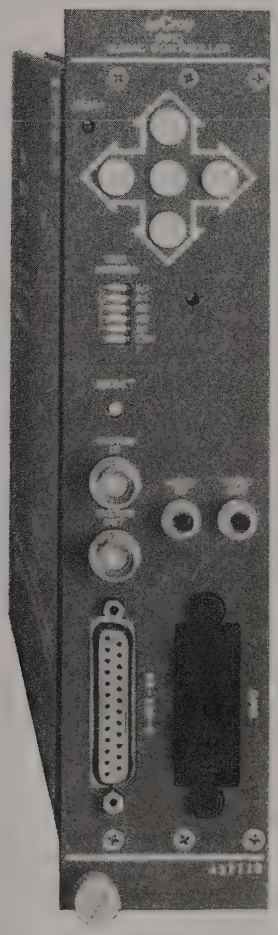


Figure 6: 6010 Interface Module

IEEE-488 Cable

An IEEE-488 cable connects the host computer to the CAMAC controller. The IEEE-488 bus contains 16 bi-directional lines to which 15 instruments (including a controller) can be connected. During operation, the bus lines transfer commands and data to and from the computer to the CAMAC controller and whatever other modules are housed in the CAMAC mainframe.

The IEEE-488 (GPIB) cables can be stacked. Therefore, connections between the host and several instruments can be in any configuration. The only user concerns are to ensure tight mating of cables by tightening hold down screws and to minimize total cable length. Increasing the cumulative cable length increases capacitance which limits bus speeds. Theoretical maximum length is 20 meters total. Practical lengths for high speed transfers should be as short as possible.

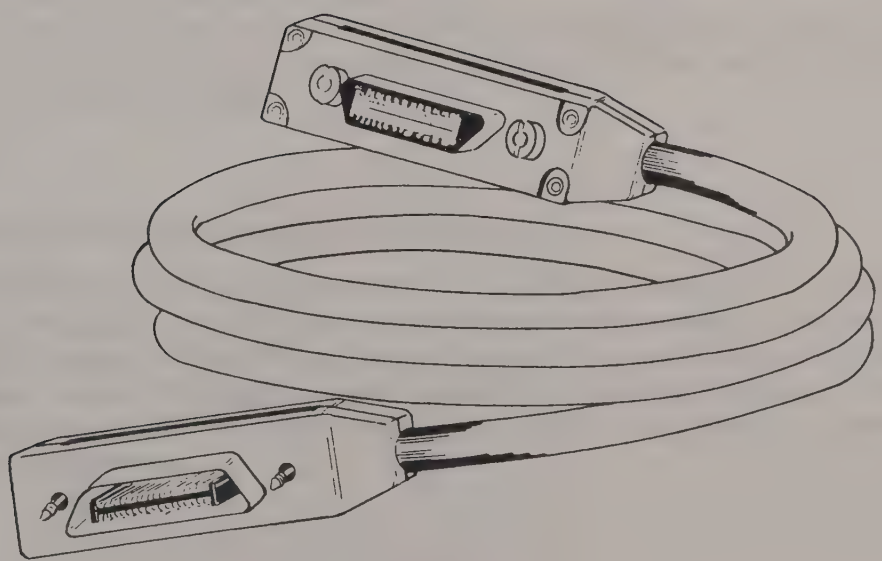


Figure 7: IEEE-488 Cable

Instrument Controller

The 8901A and 6010 interfaces are compatible with any IEEE-488 bus controller. However, when using WAVEFORM-CATALYST or ASYST Scientific Software, the Instrument Controller must be an IBM PC/XT/AT, PS/2, or Compaq III/386 (or 100% compatible).

Note: See WAVEFORM-CATALYST Operator's Manual (Version 2.6 or greater) for a list of compatible multifunction boards, graphics boards, GPIB, expanded memory boards, computers, and printers.

BASIC SETUP

BASIC SETUP is a chronological sequence of tasks for setting up a 8828D Waveform Digitizing System. It assumes that a CAMAC instrument mainframe/controller is attached to a host controller via IEEE-488 (GPIB) cable. Please review this entire section before you begin. Along with instructions for configuring the 8828D side jumpers and installing the system modules, it contains important information on slot location for correct mainframe operation and optimal component cooling. It also details the necessary cable attachments for connecting the 8828D address and data buses to the memory modules.

System setup entails seven tasks:

1. Configure the 8828D side jumpers.
2. *WITH POWER OFF*, install the 8828D in three open slots. Be sure to leave room for associated memory module(s).
3. Remove terminal resistors from all but one of the memory modules.
4. Install memory module(s) with the terminated module rightmost.
5. Set memory address switches.
6. Install either the 8901A or 6010 GPIB to CAMAC Interface Module.
7. Attach DATA #DC8150/N and ADDRESS #DC8134/N cables to the 8828D and all memory modules.

Mechanical Setup of Jumpers and Switches

The 8828D provides a choice of either TTL or ECL compatibility for both triggering and clocking. The Stop Trigger has four parameters selectable by means of side-panel jumpers: Trigger Slope, Trigger Busy and Trigger Arm Polarity, and Burst Clock Enable. The trigger level is adjustable via the front-panel potentiometer. These should be set as desired. Figure 8 shows the side panel of the 8828D and jumper selections.

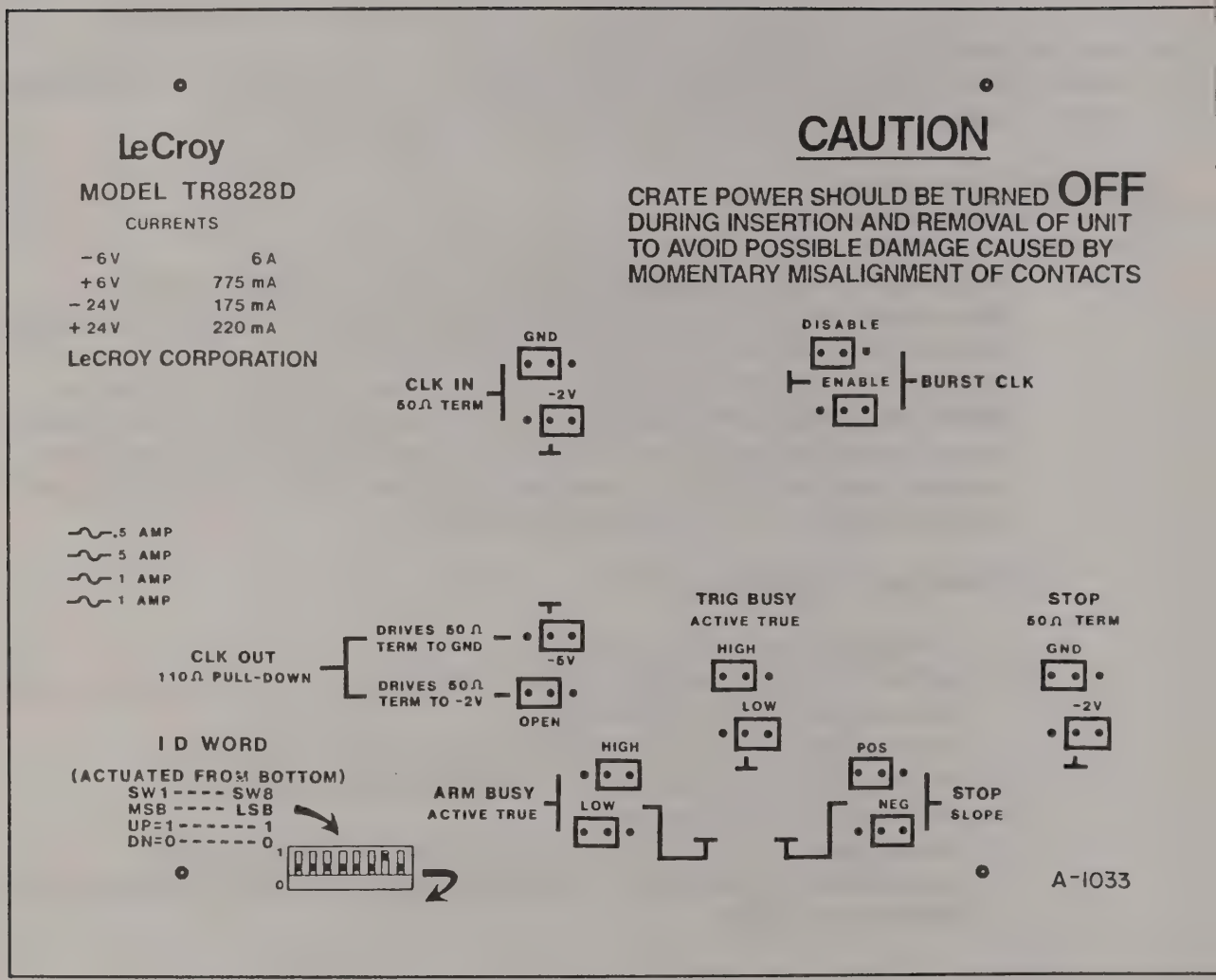


Figure 8: 8828D Side Panel

Installing the 8828D(s)

The Model 8828D Waveform Digitizer is compatible with any CAMAC mainframe which provides adequate power. *With the power off,* insert the 8828D waveform recorder in any station except the Control Station (the two rightmost locations in the mainframe), leaving room to the right for its associated memory module(s).

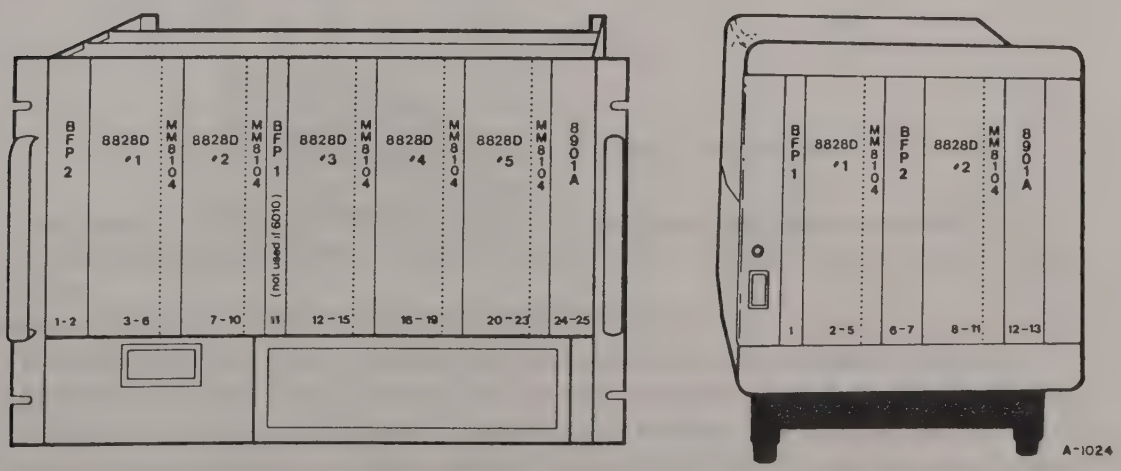
> **WARNING:** Do not attempt to install a module while the mainframe is powered on. Doing so will cause damage to its internal circuitry.

LeCroy's Model 8901A Controller requires the two rightmost slots; LeCroy's Model 6010 Controller requires the three rightmost slots.

You can install either one or two 8828D modules in an 8013A mainframe or up to five in a 1434A or 8025 mainframe when using an MM8104 memory module per 8828D (Figure 9).

> NOTE: *Page 1-5 contains specifics on attaching either the MM8103A, MM8105, or MM8106 memory modules in pairs.*

To ensure optimal cooling, install the 8828D(s) over cooling fan(s). The location of the system (CAMAC N) is defined by the number printed on the mainframe for the slot identified by an arrow on the 8828D's front panel. During bus operation the controller (GPIB to CAMAC interface) addresses this CAMAC slot to communicate with the 8828D.



As you slide the module into the mainframe, carefully align its instrument rails with the card cage. Tighten (clockwise) the thumbscrew on the 8828D's lower front panel to draw the module's interface connectors into the mainframe's backplane. Conversely, loosening the thumbscrew retracts the module's interface connectors from the backplane.

NOTE: When installing a 8828D module in a Model 8013A Benchtop Mainframe, pressing with an upward motion against the 8828D's upper front panel to slightly raise the module eases finger tightening.

Ensure that the mainframe has sufficient overhead clearance to permit adequate airflow. *Do not obstruct ventilation.* Blank front panels (Models BFP-1 and BFP-2) should be used to cover empty slot locations and thus ensure proper cooling. Do not obstruct ventilation by placing papers or other objects on the top of the mainframe.

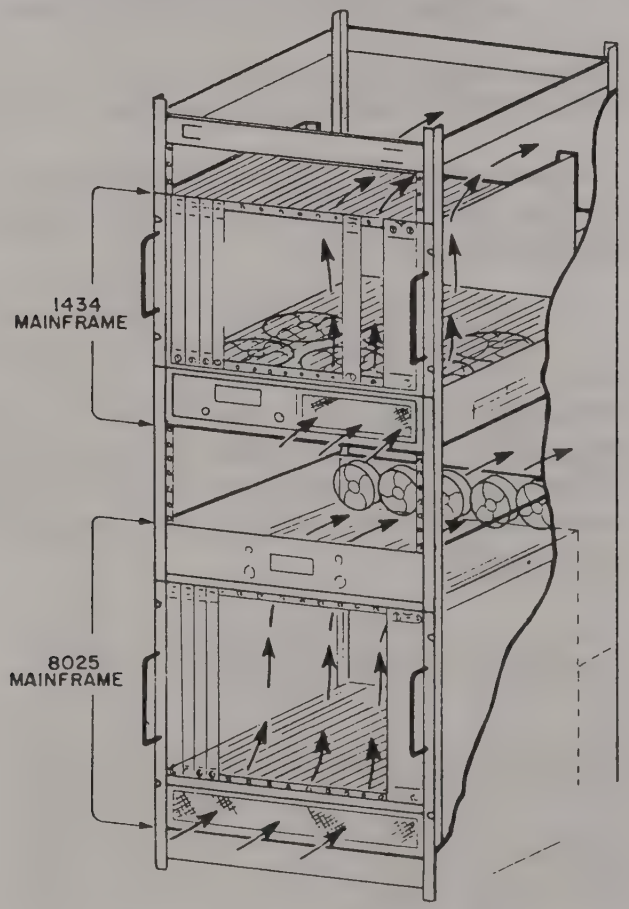


Figure 10: Airflow Path of the 1434A and 8025 Mainframes

Installing Memory Modules

Before installing the memory module(s) in the instrument mainframe, remove the resistors which terminate the 34-pin and 50-pin cable connectors from all but the last memory module. These resistors consist of seven Single Inline Package (SIP) resistor packs and a single 56Ω resistor. The resistors are located in sockets just behind the front panel and can be seen from the side of the module. See Figure 11.

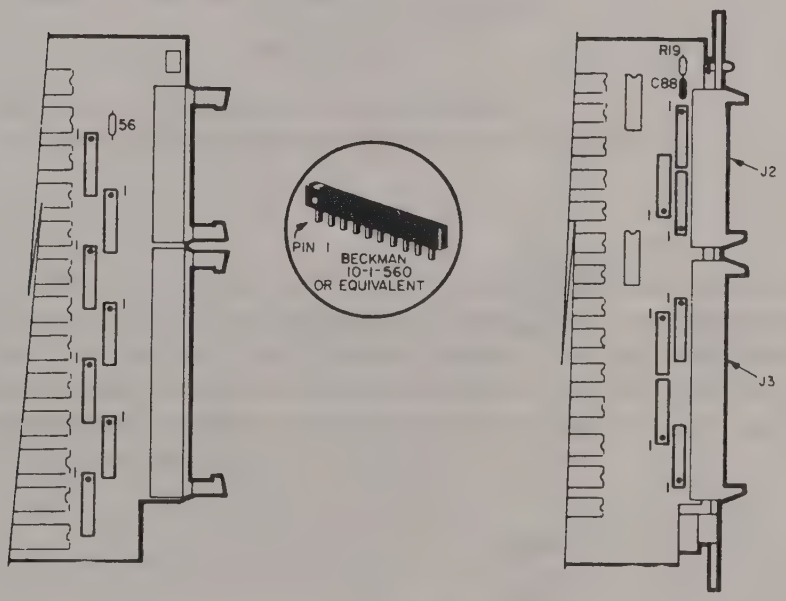


Figure 11: Termination Resistor Orientation

The memory module(s) must be installed in the instrument mainframe slot(s) just to the right of the 8828D(s). The last memory module should be the farthest to the right.

If reconfiguring a system, remove modules as required. If necessary, remove blank front panels (BFP-1 and/or BFP-2) to expose only enough open slots for the memory modules to be installed. Each memory module will occupy one slot. Modules can be removed by loosening (counterclockwise) the thumbscrew on the lower front panel until the module slides out freely. Slide each memory module into the slot until it mates with the edge connector at the back of the

instrument mainframe. Tighten the thumbscrew (clockwise) on the lower front panel to seat the module firmly.

Now the front-panel switches must be set. These binary switches set address select codes. Set the Switches as shown below for the respective memory modules.

NOTE: All additional memory plug-ins must interconnect. Be sure to order the required amount of multiple-connector ribbon cable.

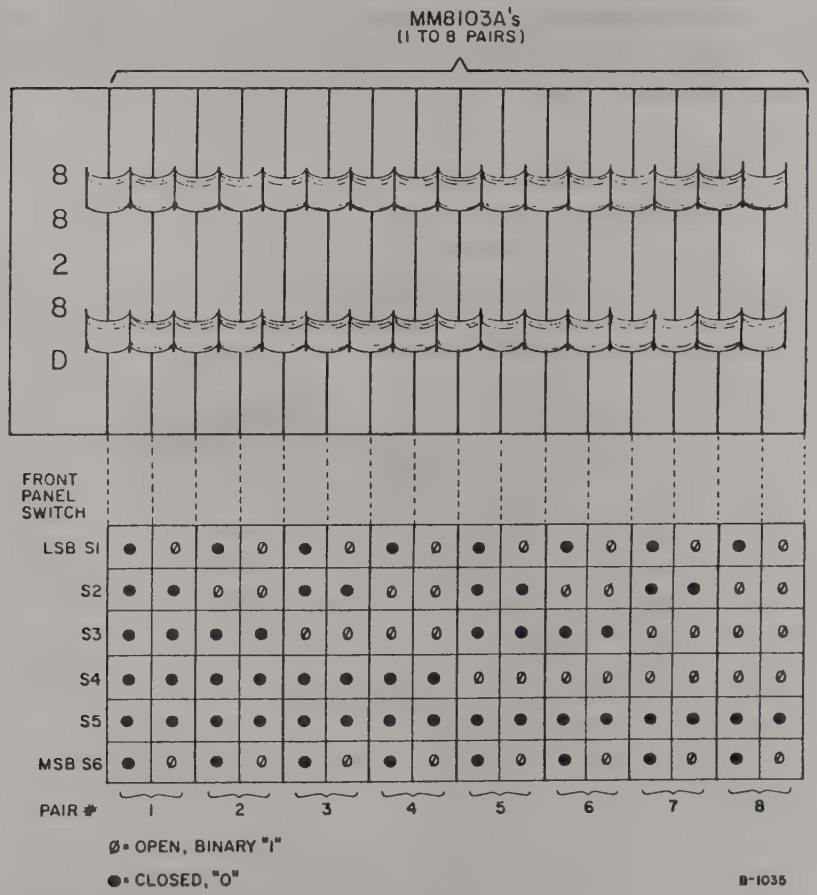
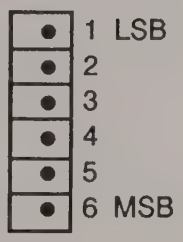


Figure 12: MM8103A Address Switch Selection

The MM8104 cannot be used in pairs. To set its address, switch its 6 DIP switches to the binary "0" or OFF position.



Ø = OPEN, BINARY "1"
● = CLOSED, "0"

Figure 13: MM8104 Address Switch Selection

The MM8104 memory module can be reconfigured to operate as an MM8103A by switching jumpers. Only when configured as an MM8103A can multiple MM8104s be used with a single 8828D. First, remove the MM8104 side panel. Next, use pliars to remove the four jumpers adjacent to the SIP Resistor Packs on the upper corner of the MM8104. Reinstall the jumpers on the lower two pins. See Figure 14 for proper jumper settings.

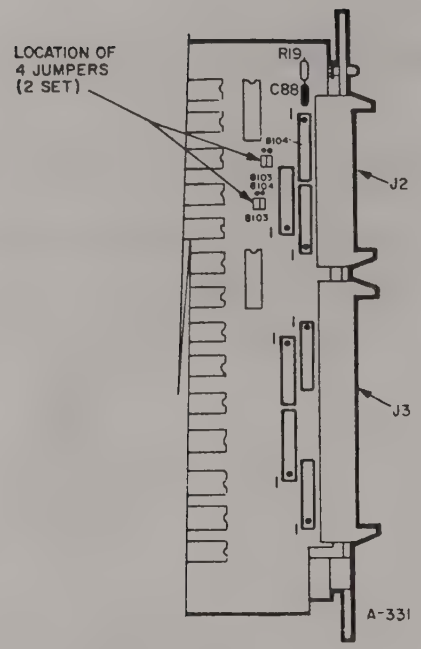


Figure 14: MM8104 Configured to Operate as an MM8103A

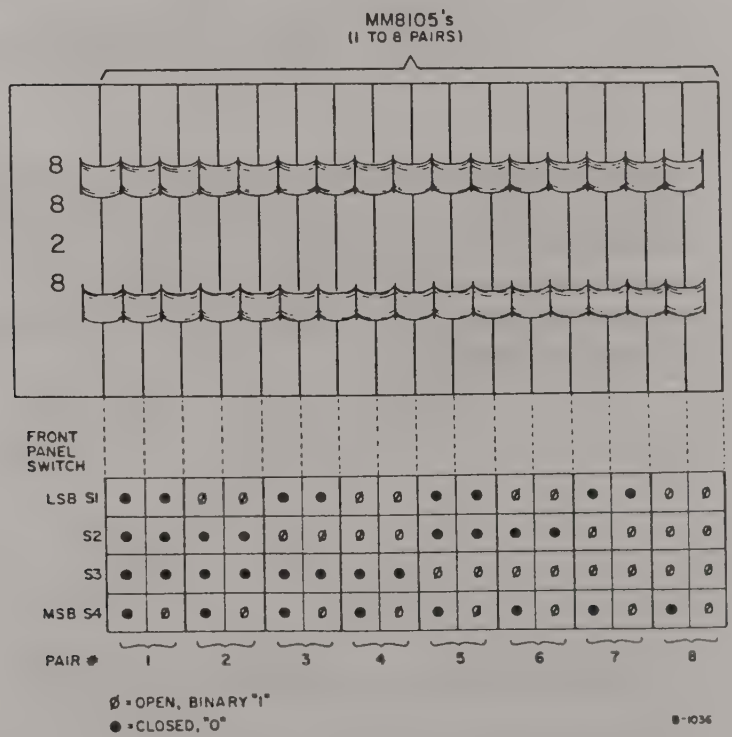


Figure 15: MM8105 Address Switch Selection

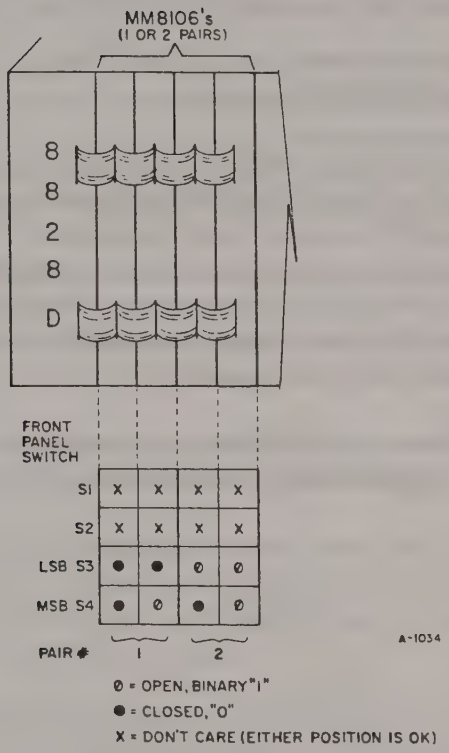


Figure 16: MM8106 Address Switch Selection

ID Word

Asserting F(3) and A(0) causes the 8-bit identification word to be read via R1-R8 of the CAMAC dataway. A switch array accessible from the bottom edge of the module allows convenient changing of the ID word. The ID word is factory set to 2, which provides Le-Croy 6010 high speed averaging compatibility.

Clock In

The 8828D Series permits the user to select the termination for the ECL level External Clock Input. This is factory set to ground termination, but may be set to -2 V termination by means of side-panel jumpers.

Clock Out

The Clock Output provides an ECL level (-.8 V to -1.6 V) signal with internal 110 Ω pulldown to -5V selectable by means of a side-panel jumper. If the internal pulldown is selected, the output will drive a

grounded 50 Ω; with the internal pulldown disabled, an external pulldown to -2 V is required.

Installing the 8901A or 6010 GPIB to CAMAC Interface Module

The rightmost slot in any CAMAC Standard mainframe is reserved for the CAMAC interface controller module.

With the power off, insert the 8901A in the two rightmost slots in the CAMAC mainframe. Tighten (clockwise) the thumbscrew on the 8901A's lower front panel. Tightening this screw draws the module's interface connectors into the mainframe's backplane. (Conversely, loosening the thumbscrew retracts the module's interface connectors from the backplane.) The 6010 module occupies the three rightmost slots in the CAMAC mainframe and is fastened by tightening (clockwise) the thumbscrew.

Interconnect the GPIB cable to the appropriate connectors on the computer and the front panel of either the 8901A or 6010 interface module.

Cabling

The 8828D requires two cables to connect the address and data buses to the memory modules. The 34-conductor upper cable connects the address bus while the shielded 50-conductor lower cable connects the data bus. These cables are kept as short as possible to minimize crosstalk and reflections.

To order cables for additional memory modules, use part numbers:

DC8134/N – 34-conductor cable
DC8150/N – 50-conductor cable

where N equals the number of memory modules to be installed. The cable will have N + 1 connectors (one extra to connect to the digitizer).

Attach the 50-conductor ribbon cable from the 8828D to each of the memory modules. Lock each header to ensure a tight connecton. A loose connection may cause erroneous data to be stored from the digitizer into memory. Repeat installation procedure for the 32-pin ribbon cable.

The input signal should be connected to either the normal input (510 mV p-p) or high level input (5.1 V p-p), and a trigger source connected to the Stop Trigger input. If it is desired to trigger on the input signal, the Fast DAC output shall be connected to the Stop Trigger Input.

Signal Conditioning

Since the 8828D has a fixed input range, the Model 6103 dual-channel amplifier and trigger generator provides signal conditioning. Each amp channel can accept low or high impedance signals over a range of 50 mV to 50 V and provide an output to drive the 8828D. The trigger generator allows programmable slope and level control from internal and external sources. When operating the 6103 with the 8828D, the signal offset should be provided by the amplifier and the digitizer offset set equal to zero. Figure 17 shows typical cabling for 2-channel operation with external trigger conditioning.

Setup of the 6103 programmable amplifier is provided by a separate setup menu when using WAVEFORM-CATALYST software.

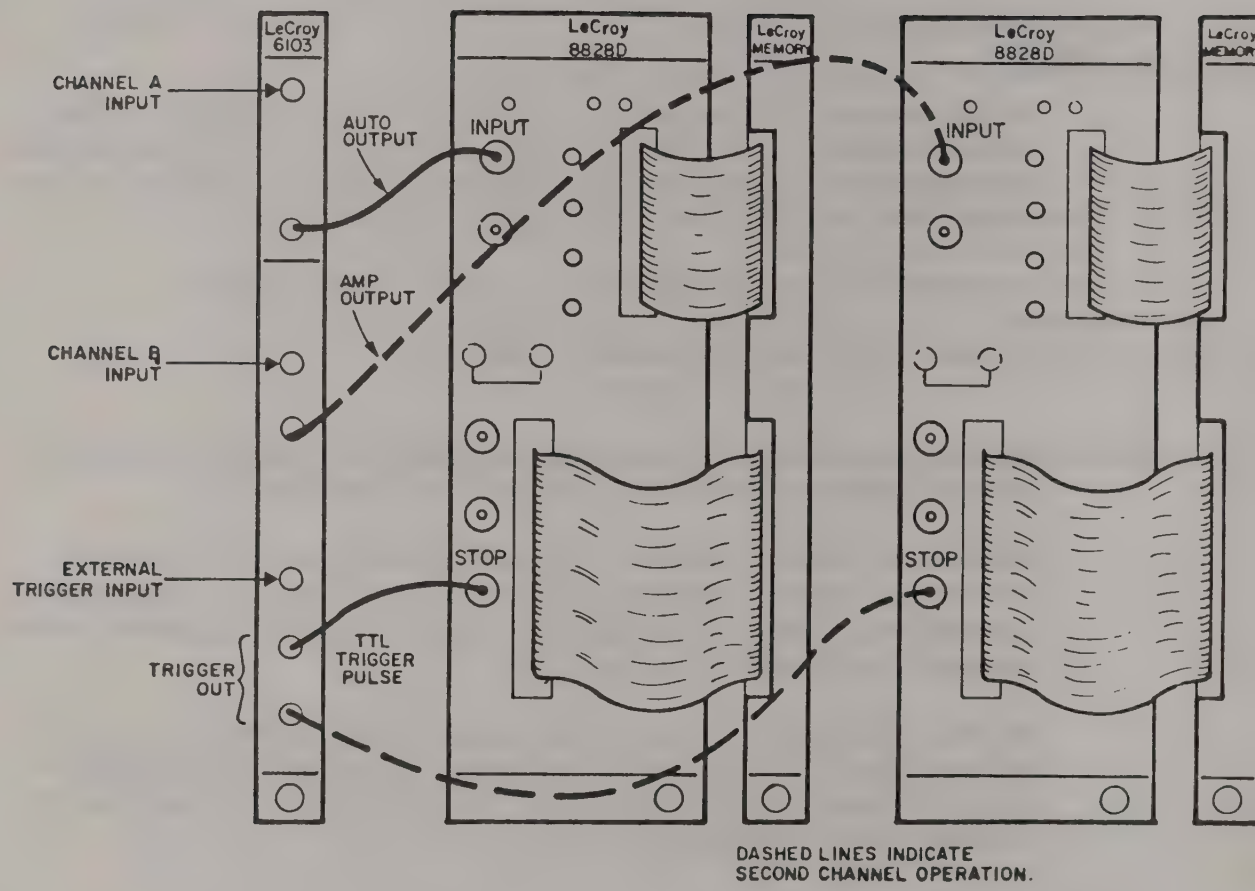


Figure 17: External Trigger Conditioning

SECTION 2: OPERATION

MODES OF PROGRAMMED CONTROL

The 8828D Waveform Digitizer is completely programmable via CAMAC. The LeCroy 8901A and 6010 Controllers employ user written programs to control the 8828D using standard GPIB protocol between the user's computer and the CAMAC instrument mainframe. LeCroy's 6010 Controller also provides an RS-232-C port for serial communication. LeCroy offers three modes of program control:

WAVEFORM CATALYST Software

Turnkey Oscilloscope emulation on an IBM PC/XT/PC/AT, PS/2, COMPAQ III/386 (or 100% compatible) using WAVEFORM-CATALYST software. LeCroy's WAVEFORM CATALYST (Model 6900) provides digital storage oscilloscope operation of the system using single keystroke commands. CATALYST sets up all 8828D operating parameters, then reads, displays, averages, histograms, stores, or prints them. CATALYST software requires either the 8901A or 6010 to be the GPIB to CAMAC interface in the instrument mainframe.

6920-DL Digitizer Driver Library

Simplified GPIB control and waveform analysis on an IBM PC/XT/AT, PS/2, COMPAQ III/386 (or 100% compatible) using LeCroy's 6920-DL Digitizer Driver Library with ASYST Scientific Software. Employing English-like command words, the LeCroy drivers make all 8828D GPIB and CAMAC commands totally transparent to the user. This software requires programming in the ASYST language. Numerous examples are included in the 6920-DL package.

GPIB / CAMAC Operation

For Automated Test Applications with non-PC host computers, GPIB/CAMAC Programmed Operation of the 8828D is demonstrated with a sequence of GPIB commands. While not specific to any controller, these commands serve as a step-by-step operation guide.

USING THE 8828D WITH WAVEFORM CATALYST™ SOFTWARE

WAVEFORM-CATALYST™ Software (LeCroy Model 6900) is an IBM-PC/XT/AT, PS/2, COMPAQ III/386 (or 100% compatible) based digital storage oscilloscope software package for LeCroy modular recorders, including the 8828D digitizer. *(Note: hereafter, text references to CATALYST are synonymous with WAVEFORM CATALYST.)* The software communicates with the 8828D via the 8901A or 6010 controller and the GPIB. It provides control, display, manipulation, and archiving of digitized data. Single keystroke commands make the system easy to learn and to use. No prior knowledge of computers, programming or interface standards is required. Figure 18 shows the waveform display generated by CATALYST software and the 8828D waveform recorder. Up to 4 waveforms can be simultaneously displayed.

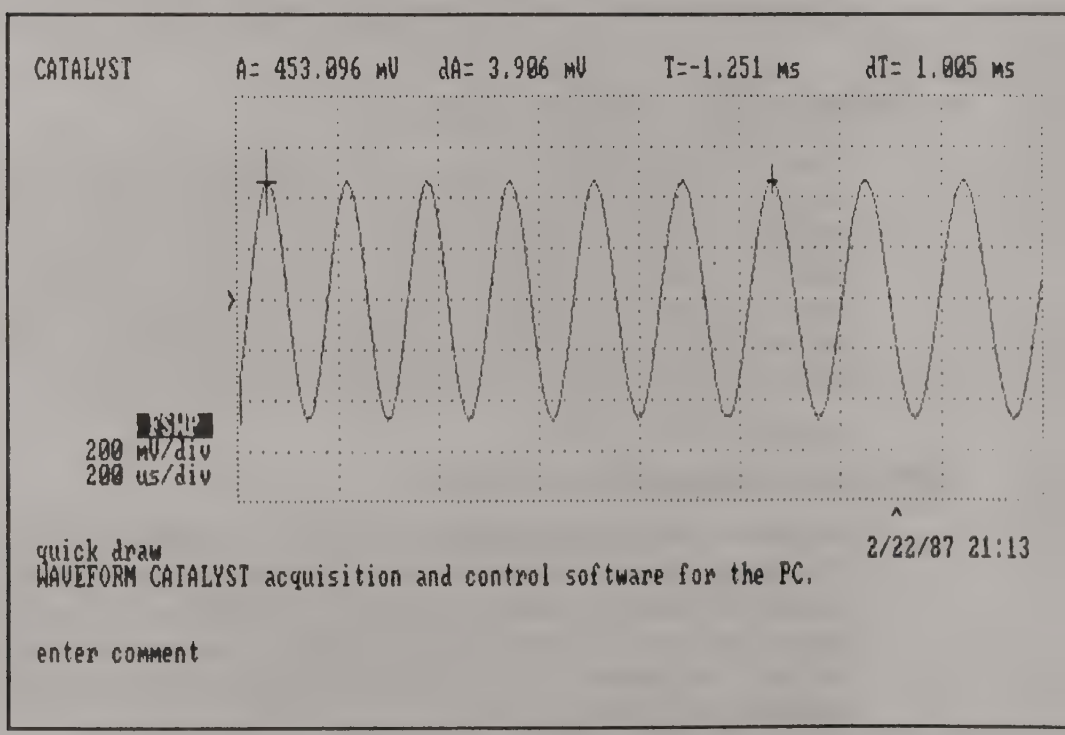


Figure 18: Generated Waveform

Using the 8828D with WAVEFORM-CATALYST Software

To run the 8828D with CATALYST software, first refer to the WAVEFORM-CATALYST User's Manual for a guide to configuring and assembling the personal computer and properly loading the software.

CATALYST Software can control up to 100 digitizer channels and up to 10 different digitizer types. Each instrument mainframe (8013A , 1434A, or 8025) can house multiple digitizing modules according to available space and power. CATALYST operation is identical whether using the Model 8901A or the 6010 GPIB controller.

You should become familiar with software commands executed from the PC keyboard by referring to the CATALYST Quick Reference Card or by pressing **F1**. Most of CATALYST's primary commands use single keystrokes; that is, only the key corresponding to the first letter of the command must be pressed in order to execute that function. For instance, if the modules in your system are configured properly, pressing **A** selects "Auto Trigger" mode which repeatedly "arms" and triggers the module.

Some commands require additional information, in which case CATALYST prompts the user for it. An example is WRITE DATA command. When **W** is pressed, the message "enter file name:" is displayed.

For a few commands, a menu of sub-commands is displayed in the lower screen. While the menu is displayed, any of its commands can be entered by pressing the key which corresponds to its first letter. Pressing the **space bar** erases the command menu and returns the keys to their primary functions. **G** is an example of this command type since it activates the "Grid Format" menu.

CATALYST Example

The following example illustrates a sequence of CATALYST commands used to acquire and display data from a LeCroy 8828D 200 megasample/sec digitizer which has been placed in slot 5 of the instrument mainframe. The GPIB address on the 8901A or 6010 has been set to 1 on the front-panel DIP switch.

Install CATALYST to your floppy or hard disk using setup instructions in the CATALYST manual. When CATALYST is loaded, choose digitizing parameters as follows:

COMMAND	RESULT
L	Pressing the **L**(ist modules) key causes the available system modules to be listed in the lower screen. Select the number of the module you want to operate.
3	In our example **3** is the number which represents the 8828. Pressing it causes the Setup menu to appear.

SETUP MODULE TR8828

		A	B	C	D	E	F	G	H	I	J
1	NAME	1828									
2	ACQUIRE	YES	NO	NO	NO	NO	NO	NO	NO	NO	NO
3	STORE	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
4	PROCESS	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO
5	GPIB ADDR	1									
6	SLOT	5									
7	PERIOD ns/pt	5	5	5	5	5	5	5	5	5	5
8	MEM SIZE (k)	1	32	32	32	32	32	32	32	32	32
9	PTS 1/8's	0	0	0	0	0	0	0	0	0	0
10	OFFSET (mv)	0	0	0	0	0	0	0	0	0	0
11	FULL SCALE V	.512	.512	.512	.512	.512	.512	.512	.512	.512	.512
12	EXT PERIOD										
13											
14											
15											

All modules Enter Goto Help Next Previous Read Write
press space to return

E	Use the arrow keypad (left, right, up, down) to move reverse video on screen to digitizing parameter you wish to modify. Then press **E** key to select it.

NOTE: after changing a parameter's setting, press ↵ (ENTER or RETURN KEY). Always press **E** *to select the highlighted parameter for modification, and always press ↵ following the modification.*

Set the following parameters as follows:

NAME	**TR28**
ACQUIRE	**YES**
GPIB ADR	**1**
SLOT	**5**

Setting the above parameters as indicated will configure the system to acquire data.

W (Optional) You can store your setup using **W**(rite) in the SETUP menu. Selecting the file name **SD8828.CAT** causes the current menu values to be loaded automatically each time CATALYST is begun. Pressing the **<SPACE BAR>** exits the SETUP menu and initializes the 8828D with the values on the SETUP menu.

Connect input signal and trigger input (STOP on 8828D front panel) cables.

Next, select which trace to display:

1 Pressing **1** selects the bottom Trace. Traces are numbered from 1 to 4 from the bottom to the top of the screen. CATALYST prompts for name of channel to be displayed.

TR28 Enter four digits corresponding to name of module as defined in SETUP menu.

G Pressing **G**(rid) allows you to select how many grid boxes you want (**S**ingle, **D**ual, or **Q**uad). If you have multiple traces displayed, this function permits you to display them separately or overlayed. Select **S** for single grid.

A **Press A**(uto) to select CATALYST automatic triggering mode. The 8828D will digitize a waveform once every 3 seconds with the parameters you have selected. CATALYST will display the waveform and continuously update the screen with fresh 8828D data.

The trace may be expanded, positioned, and operated upon with cursors. Reverse video on channel name (at left of screen) indicates which trace CATALYST keys are operating on.

F To speed expansion, positioning, or cursor movement, press **F** to freeze the trigger. You may acquire a new waveform by pressing **A** again.

NOTE: if you have more than one channel operating, each memory must be read out before any recorder can be re-armed. The active trace is selected by moving the primary cursor (selected by pressing the **Home** *key) up and down.*

To turn off an undesired trace, press the trace number you wish to remove. When prompted for trace name, press ↵ (ENTER or RETURN) without entering any text.

The screen should now be updating with data from the 8828D. Select other triggering modes **N**(ormal), **S**(ingle), **M**(anual) respectively. Other CATALYST functions are highlighted in the user's manual and on the CATALYST user's card.

You can access the "help" screen for the 8828D by accessing the 8828D setup menu and pressing **H**. The following menu will appear:

8828D – 200 MSample Transient Recorder

8 bit resolution
up to 2M memory (512k for all units before ECO# 2005)
512 mv peak-to-peak signal range

Notes:

1. If an external clock is used, the PERIOD must be set to EXT and the EXT PERIOD must be set so that the time scale will be a correct valid range, 10 nsec to 9999 ns.
2. Offset range is –256 mv (unipolar positive signal) to 256 mv (unipolar negative signal).
3. Full scale volts is provided as a correction factor for amplitude in case an amplifier or attenuator is used. Valid range is .1 mv to 100 v.
4. The first and last 16 samples may have been overwritten and are therefore set to zero so that erronious data will not be displayed.
5. Pre-trigger sample size (PTS) ranges from 0 to 8 eighths of memory.
6. Data is displayed in blocks of 8k words. Multiple blocks may be viewed simultaneously by assigning the module to more than one trace and paging to the desired blocks.
7. Memory size is selectable in 16k steps up to 2 Megawords. It is possible to read in and store less than 16k points but 16k points will be sampled.

press any key to continue

Figure 19: WAVEFORM-CATALYST 8828D Help Screen

Additional Help screens like the one pictured in Figure 19 are available for each module type in the LIST MODULE menu. To access these help files, enter the SETUP Menu and press **H**(elp).

When used with the 6103 programmable amplifier, gain, offset, and triggering can be controlled by the separate setup menu for the 6103. For proper voltage/division and delta voltage cursor readouts on the display screen, be sure to enter the FULL SCALE V setting in the 8828 EDIT menu to A, N or B, N where A or B represents the 6103 amplifier channel and N represents the 6103 installed slot number (e.g., 1, 2, 3, ...).

Using the 8828D with ASYST/LeCroy Drivers

The LeCroy Model 6920-DL Digitizer Library simplifies data acquisition, storage, and complex waveform analysis using the 8828D Waveform Digitizer. Employing English-like command words, the LeCroy drivers make all GPIB and CAMAC commands totally transparent. The LeCroy drivers are fully integrated with the ASYST™ language. You go smoothly from data acquisition to analysis to graphics–all with the same system, using a single set of protocols, user interfaces, and documentation. So you spend less time writing code and more time on your research.

The 6920-DL Drivers consist of high and low level commands. High level commands control functions that are specific to individual digitizers. Commands corresponding to each LeCroy Digitizer (and LeCroy's 6103 Amplifier Module) are stored in separate system overlays. Therefore, if your system contains the 8828D, only its relevant overlay need be loaded, thus conserving valuable data array space.

Low level commands address functions common to many modules. Also, they send CAMAC commands to modules in the mainframe. This allows modules not supported in the 6920-DL package to be programmed.

Typical Command Sequence

The following example steps you through a typical command sequence to acquire and display data from a single 8828D.

Step 1: Configuring the ASYST™ System

Prior to 6920-DL system operation, ASYST must know which GPIB card is in the PC, as well as the CAMAC controller model and digitizer(s) currently in use. LeCroy drivers are compatible with any GPIB cards supported by ASYST™ and with either LeCroy's 6010 or 8901A Interfaces. For our example, we chose the 8901A. (Notice that when typing in commands, only "8901" is entered. Similarly, commands which address the 8828D are entered as 8828.)

Step 2: Defining the Controller's Parameters

The **CAMAC.CRATE** command is used to define the CAMAC Controller parameters. Our example uses an 8901A controller set for GPIB Address #1 (Controller front panel DIP setting A0 "on," A1 through A4 "off"). The command expects two parameters on the ASYST memory stack before executing. The GPIB address (1) must be placed on the stack first followed by the CAMAC Controller model number (8901):

OK 1
OK 8901
OK CAMAC.CRATE

Step 3: Defining which Digitizer to use

Each LeCroy digitizer has an "N" printed on its lower front panel. When the digitizer is placed in a CAMAC crate, the arrow beneath the N points to a number on the crate. This number, referred to as the "CAMAC N Slot Number," is the digitizer's address. This address is used to communicate with the digitizer over the CAMAC bus. Our 8828D has a CAMAC N Slot Number of 3:

OK 3
OK CAMAC.SLOT

Step 4: Initializing the Drivers

Before sending any data over the GPIB, the Drivers must be initialized and the PC must be made the controller in charge. This is accomplished using the INIT.CAMAC command.

OK INIT.CAMAC

Step 5: Setting the Digitizer's Parameters

The digitizer's sampling rate, pretrigger size, memory size, and analog input offset are set using 8828.CONTROL.WORD and 8828.OFFSET commands.

Example: Pretrigger size = 16K (**4/8ths** of memory)
Sampling rate required = **5 ns** per point (200 megasamples/sec)
Active Memory size = **32 ksamples**

```
OK 4
OK 5
OK 32
OK 8828.CONTROL.WORD
OK 0
OK 8828.OFFSET
```

Step 6: Arming and Triggering the Digitizer

The digitizer, now ready to acquire data, is "armed" using 8828.ARM command. The 8828D will accept a trigger only after arming. A trigger can be supplied externally using the digitizer's STOP input, or manually using 8828.TRIGGER command.

Example: Arm module and supply a manual trigger

```
OK 8828.ARM
OK 8828.TRIGGER
```

Step 7: Extracting Data

Prior to extracting data from the 8828D digitizer, an ASYST DMA array must be dimensioned to store it. This is accomplished using the ASYST command "DIM[nnnn] DMA.ARRAY name". Next, the digitizer is prepared for readout using the 8828.ENABLE.READ command. Data is read out and into the array using the 8828.READ.DATA command.

Example: Dimension a 1K point array and read out data

```
OK  DIM[ 1024 ] DMA.ARRAY TEST
OK 8828.ENABLE.READ
OK TEST
OK 8828.READ.DATA
```

Step 8: Plotting the Data

Once the data is in the ASYST environment, the powerful ASYST commands simplify plotting and analysis. A basic example of graphing g a digitized waveform to the PC screen follows:

```
OK Y.AUTO.PLOT
```

The complete example follows:

```
OK 1
OK 8901
OK CAMAC.CRATE
OK 3
OK CAMAC.SLOT
OK INIT.CAMAC
OK 4
OK 5
OK 32
OK 8828.CONTROL.WORD
OK 0
OK 8828.OFFSET
OK 8828.ARM
OK 8828.TRIGGER
OK DIM[ 1024 ] DMA.ARRAY TEST
OK 8828.ENABLE.READ
OK TEST
OK 8828.READ.DATA
OK Y.AUTO.PLOT
```

GPIB / CAMAC Programmed Operation of the 8828D

This section provides a sequenced guide to programming the 8828D and interpreting the decimal control words. For background reading, refer to Appendix B of this manual or to LeCroy AN-33, *Introduction to CAMAC*.

Power Up

After applying power to the waveform digitizer and memories, a Z (reset) command should be issued to set the modules to a known state.

Setting Control Word

The control register contains the user bit, memory size, sampling period, and pretrigger size in the following format. Because the control register has battery back-up, it will always contain the last control word written to it. When the waveform digitizer is not in the "armed" state, the control word may be read and changed using the F(0) and F(16) CAMAC functions.

The control register is 16 bits in length. It is programmable by asserting F(16) A(0) W(n) on the CAMAC dataway Write lines W1 through W16. Asserting F(0) A(0) on the CAMAC dataway reads the control register onto the CAMAC dataway Read lines R1 through R16.

W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1
R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
U0	M6	M5	M4	M3	M2	M1	M0	X	S2	S1	S0	P3	P2	P1	P0

Where U0 is the user bit
M0, . . . M6 is the memory size
X not used, state does not matter
S0, S1, S2 is the sampling period
P0, P1, P2, P3 is the pretrigger size

The control register is decoded as follows:

Binary							Decimal	Value
M6	M5	M4	M3	M2	M1	M0		
0	0	0	0	0	0	0	0	16K bytes
0	0	0	0	0	0	1	1	32K bytes
0	0	0	0	0	1	0	2	48K bytes
0	0	0	0	0	1	1	3	64K bytes
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	127	2048K bytes

		S2	S1	S0	
		0	0	0	0	5 nsec
		0	0	1	1	10 nsec
		0	1	0	2	20 nsec
		0	1	1	3	40 nsec
		1	0	0	4	80 nsec
		1	0	1	5	160 nsec
		1	1	0	6	320 nsec
		1	1	1	7	external clock

	P3	P2	P1	P0	
	0	0	0	0	0	0/8 of memory
	0	0	0	1	1	1/8 of memory
	0	0	1	0	2	2/8 of memory
	0	0	1	1	3	3/8 of memory
	0	1	0	0	4	4/8 of memory
	0	1	0	1	5	5/8 of memory
	0	1	1	0	6	6/8 of memory
	0	1	1	1	7	7/8 of memory
	1	0	0	0	8	8/8 of memory

P0-P3 set the pretrigger size, the fraction of the selected memory size that will precede the STOP command. For example, if a memory size of 32K and a pretrigger size of 3/8 are selected, then after a digitizing cycle, the first 12K bytes of memory will contain data sampled prior to the STOP command and the last 20K bytes the data sampled after the STOP command.

S0-S2 set the period of the sampling clock. As shown above, you may choose any of seven internal periods or an external period. The external clock signal should have a 50% duty cycle.

WARNING: If external clock mode is selected, once "armed" the 8828D *must see* an external clock signal before it can be removed from external clock mode, triggered, or before data can be read out.

M0-M6 set the size of the data record. These bits select any memory size from 16K to 2M in 16K increments. The data record represents activated waveform, not installed waveform memory.

The user bit **U0** can be set and read. This bit has no internal function so it can be used for storing status, run number, etc., by the user.

The definition of the control word using decimal notation for the control bits is:

$$CW = PD + (SD \times 16) + (MD \times 256) + (UD \times 32{,}768)$$

For example, for 16 ksamples of active memory, 5 nsec sample interval, 5/8 of memory pre-trigger, and user bit set to zero, the unique decimal value of the control word is:

$$CW = 5 + (0 \times 16) + (0 \times 256) + (0 \times 32{,}768) = 5$$

Setting Offset

Analog signals at the input to the 8828D may be offset by 255 mV with the offset register. The offset

register is also battery backed-up and will contain the last value of offset written to it. The offset register is 8 bits in length and is programmed via the CAMAC dataway. Asserting F(19) A(0) W(n) will write to the offset register on CAMAC dataway Write lines

W1 through W8. Asserting F(1) A(0) will read back the offset register on CAMAC dataway Read lines R9 through R16.

Writing 0 to the offset register allows input signals between ground and -510 mV to be digitized. An offset of 127 allows signals between -255 mV and +255 mV to be digitized. An offset of 255 allows signals between ground and +510 mV to be digitized. Intermediate value of offset will displace the input signal correspondingly.

Measuring the signal at the fast DAC output can assist in determining the optimum offset level. Actual offset will differ from the programmed request by less than ±2% of the full scale (±5.0 counts). If 2% accuracy is not sufficient, the user can obtain the exact number of offset counts desired by writing an offset, reading back the actual offset, and then adjusting the requested offset to obtain the desired final offset.

Offset	Range of Input	Use
0	–510 mV to 0 mV	negative signal
127	–255 mV to +255 mV	bipolar signal
255	0 mV to +510 mV	positive signal

The DC level of the input can have some effect on accuracy. If the input is biased to the exact center of full scale, then it will toggle between outputs of 10000000 and 01111111. In all cases the RMS variation of the output will be less than two counts; typically the RMS variation is less than one count. This situation (with all bits toggling) will generate enough noise to cause a measurement error. To avoid these

errors, the user should not apply a DC level to the input (or request an offset) corresponding to 127 counts. Similar but smaller effects may be observed at other DC input levels which correspond to the toggling of many bits (e.g. 63 counts).

When using the 6103 programmable amplifier, set the offset at the amplifier and keep digitizer offset equal to zero.

Sampling the Waveform

Once the pretrigger, sampling period, active memory size, and offset are set to desired values, input waveforms can be recorded. The F(9) command arms the 8828D. Once armed, the 8828D begins converting waveforms into digitized data and the memory begins storing data in a circular fashion. The waveform recorder fills the memory sequentially. Upon reaching the end of memory (length set by the control word), the recorder starts at the beginning and writes over old data. Acquisition will continue until a stop trigger is received.

Only the stop command, F(25) A(0), the STOP TRIGGER input, or the initialize signal Z can remove the 8828D from the armed state. Only one CAMAC function code command will be recognized, F(25) A(0). All others will be ignored and will generate Q = 0. The trigger level for the front panel STOP TRIGGER input is adjustable ± 2 V via the front-panel potentiometer and may be monitored via the test point. When operating in the external clock mode, a stop trigger will not be recognized unless an external clock is being supplied. Until this occurs, the unit will disable all CAMAC commands.

LAM Interrupt

Following receipt of the trigger, the waveform recorder continues operation until the selected number of post-trigger samples have been digitized and stored. The internal LAM is then set. If enabled via F(26) A(0), LAM will be asserted on the dataway. LAM can be cleared via F(10) A(0) or Z. Asserting

F(9) A(0) and starting a new digitizing cycle will also clear the LAM.

To determine if acquisition has finished, the LAM or LAM status can be tested with F(8) or F(27) respectively. An alternative to polling the LAM is to enable the LAM with F(26) before starting to sample and then using the crate LAM to interrupt the processor with a service request.

Data Readout

Digitized data can be read from the memory modules via commands sent to the 8828D. Asserting F(17) A(0) will load the starting address of the data in memory from an internal register into the address counter. This starting address pointer is necessary due to the circular memory architecture (i.e., every waveform acquisition may have a different Stop Trigger location in memory. The waveform data can then be read by generating successive F(2) A(0) commands. Q will be true (Q = 1) for every valid data sample. After the last sample is read, further F(2) A(0) commands will produce Q = 0.

The memory is battery backed up. Therefore, even if line power fails during readout, the data can be read again. Assert F(17) A(0) to reload the starting address and then use F(2) A(0) to read the data.

Data is read sequentially from the memory modules, 2 bytes at a time. Dataway Readlines R1-R8 contain the first byte and R9-R16 contain the second. This 2-byte readout maximizes the transfer rate to a host computer.

The first word (R1–R16) that is read with F(2) A(0) after F(17) A(0) is a status word. If this status word is zero, then the first byte (R1–R8) of the next word is the first byte of the data record. If the status word is a one, the second byte R9–R16 of the next word is the first byte of the data record, etc. Because the data bytes are pipelined into the memory, the first

and last 16 bytes of the data record will contain invalid data.

The outstanding reliability of data provided by the 8828D is carefully checked by the factory. Prior to shipment all units undergo thorough testing, including operation during temperature cycling and at the maximum specified temperature. Tests include the digitization of slow ramp signals and many frequencies of sine waves. The output is then compared with the known input. On very rare occasions a signal data word will have a bit error. A particular bit which should be on may be off or vice-versa. All flash ADC based systems produce this type error near their maximum conversion rate. All 8828D units are factory checked for a conversion error rate. The 8828D typically produces less than one wrong data sample per million data words using a 1-million sample test.

Abbreviated CAMAC Programming Guide

The following CAMAC commands are suggested for controlling the 8828D module.

SETUP:	F16 A0 Wd	Program control register, value 'd'
	F19 A0 Wd	Program offset register, value 'd'
READY:	F26 A0	Enable LAM
	F9 A0	Arm
TRIGGER:	F25 A0	Trigger
CLEAR:	F10 A0	Clear LAM
	F24 A0	Disable LAM
READ:	F1 A0	Read back offset register
	F0 A0	Read back control resister
	F17 A0	Prepare to read
	F2 A0	Read block of data

Sample FORTRAN Program

The following FORTRAN program illustrates the use of the 8828D and Memory Modules. The program uses subroutines called CAMO and CAMI every time a command is transferred to the instrument mainframe and digitizer:

```
C example program for the 8828D Series
      PROGRAM SAMPLE
C the subroutine CAMO executes one CAMAC cycle
C the parameters for the subroutine
C CAMO (SLOT,F,A,W) are
C          SLOT   for which N is asserted
C          F      value of function code to be asserted
C          A      address to be asserted
C          W      data written to W1-W16

C the subroutine CAMI executes one CAMAC cycle
C the parameters for the subroutine CAMI(SLOT,F,A,X,Q,R)
C are
C          SLOT   for which N is asserted
C          F      value of function code to be asserted
C          A      address to be asserted
C          X      value of X returned (true or false)
C          Q      value of Q returned (true or false)
C          R      data read from R1-R16

C the subroutine CRATE sets crate address to the value of the
C argument
C the subroutine PULSEZ generates a common Z to the
C addressed crate

      INTEGER SLOT,MEM,PERIOD,PRETRG,USER
      INTEGER CONTRL,OFFSET
      INTEGER PNTR,TEMP,DATA(1024)
      LOGICAL X,Q

C address waveform recorder in slot 10 of crate 1
      CALL CRATE(1)
      SLOT = 10
```

```
C pulse Z reset line to reset waveform digitizer
      CALL PULSEZ
C set memory size to 16K (range 0-31)
      MEM=0

C set sampling period to 5nsec (range 0-7)
      PERIOD=0
C set pretrigger samples to 4/8 of memory size (range 0-8)
      PRETRG=4

C set user bit to 1
      USER=1

C write to control register using F(16) A(0) to set memory
C size, sampling period, pretrigger samples, and user bits.
      CONTRL=USER*32768+MEM*256+PERIOD*16+PRETRG
      CALL CAMO(SLOT,16,0,CONTRL)

C set input offset to center 0 V input (range 0-255)
      OFFSET=128

C write to offset register with F(19) A(0)
      CALL CAMO(SLOT,19,0,OFFSET)

C start sampling and reset LAM with F(9) A(0)
      CALL CAMO(SLOT,9,0,0)

C issue stop command, F(25) A(0), then check for LAM
C if LAM is not set (meaning that the record is not finished),
C then issue another stop and check LAM again...

C the additional stops are required because the stop trigger is
C disabled during the first cycle through the memory to
C insure that the pretrigger samples are written

100 CALL CAMO(SLOT,25,0,0)
      CALL CAMI(SLOT,27,0,X,Q,TEMP)
      IF(.NOT.Q) GOTO 100

C load starting address into memory address counter
C and initialize data read-out with F(17) A(0)
      CALL CAMO(SLOT,17,0,0)
```

```
C read status word to get pointer to first valid data byte
C add 16 to pointer so that garbled bytes are skipped
      CALL CAMI(SLOT,2,0,X,Q,PNTR)
      PNTR = PNTR + 16

C read waveform data (1024 bytes) using F(2) A(0)
      DO 200 I = 0,511
         CALL CAMI(SLOT,2,0,X,Q,TEMP)
C get data byte from R1-R8
         DATA(2*I + 1) = TEMP.AND.255
C    get data byte from R9-R16
200      DATA(2*I + 2) = (TEMP/256).AND.255

C the array DATA now contains 1024 8-bit samples
C with values of 0 to 255
C the PNTR points to the first valid sample

      STOP
      END
```

PROGRAMMING VIA 8901A AND 6010

The following is a condensed outline of commands to assist a first time user of LeCroy's 8828D Waveform Digitizer in combination with the LeCroy Model 8901A CAMAC to GPIB interface. Programming requires the use of CAMAC Function (F) subaddress (A), and mainframe slot (N) codes. When programming GPIB operation, the LeCroy 8901A is programmed in decimal codes, while the 6010 provides an ASCII command structure with multiple options and high speed signal averaging.

The following information is just sufficient to operate the system, assuming the user is generally familiar with the GPIB controller (computer) being used. Individual manuals and technical data sheets on these modules as well as IEEE-583 CAMAC and IEEE-488 GPIB Standards should be used to obtain a more thorough understanding of the system.

8901A Guide

For purposes of this example, assume that the Model 8901A is at GPIB address 1 and the Model 8828D is in slot 3. The operations that will be performed are:

Initialize the instruments upon power on and initiate sampling,
Wait for trigger,
Enable 8828D for reading,
Read data out in high-speed mode, and
Read acquisition parameters.

The implementation of this sequence (from the GPIB system controller) is given below. Since programming languages and GPIB computers use different formats for GPIB commands, the following generic notation is used throughout the 8901A programming example:

OUT x,y,...	Indicates a transfer from the GPIB controller to the 8901A. It includes addressing the 8901A to Listen, sending the data byte(s) to it, and then sending the GPIB Unlisten command.
N B1,...Bn,R	Indicates a n + 1 byte transfer from the 8901A to the GPIB controller. It includes addressing the appropriate 8901A to Talk, reading the data byte(s) into the computer, and then sending the GPIB Untalk. (B1 ... Bn) are data bytes; R is the CAMAC response byte containing X and Q.
TALK	Indicates sending out the GPIB Talk address to the specific 8901A. This is used to execute a CAMAC cycle when no data is to be returned. The IN command may be substituted if desired (e.g., to allow monitoring the CAMAC response bits X and Q).

The following shows segments of a control program using the LeCroy 8901A and the 8828D. The sequence from initialize through data readout is outlined.

Initialize the Instruments

OUT 33	Initialize the crate by sending CAMAC Z.
TALK	Execute CAMAC cycle by addressing 8901A to Talk.
OUT 98	Program 8901A to return 16 bits of data and the CAMAC response byte.
OUT 16,0,3,D1,D2	Program instrument's parameters by sending F(16) A(0) N(3) W(D1) W(D2) [D1, D2 are the parameter bytes].
IN B1,B2,R	Execute CAMAC cycle and get CAMAC response.
OUT 19,0,3,D1	Program offset in 8828D to value D1 by sending F(19) A(0) N(3) W(D1).
IN B1,B2,R	Execute CAMAC cycle and get response.

Enable LAM

OUT 65	Program 8901A to set SRQ on LAM.
OUT 26	Enable 8828D to generate LAM by sending F(26) (Note that since the A and N have not changed it is not necessary to resend them).

Initiate Sampling

OUT 9,0,3	Initiate sampling in the 8828D with a F(9) A(0) N(3).

Wait for Trigger

At this point, the 8828D is waiting for a trigger [either external or from an F(25) A(0) sent to it]. After the trigger occurs and the module is finished acquiring data, it will generate a service request (LAM). Perform a serial poll to determine which instrument set LAM (assuming there is more than one).

OUT 64	Disable the 8901A from generating another SRQ.
SPE	Send the GPIB serial poll enable command.
IN R,L1,L2,L3,L4	Read in the 5 status bytes (R is the CAMAC response byte and L1 – L4 are the current state of the LAM lines).
SPD	Send the GPIB serial poll disable command.

Enable 8828D for Reading

OUT 10,0,3	Clear LAM in 8828D with F(10) A(0) N(3).
TALK	Execute CAMAC cycle by addressing 8901A to Talk.
OUT 17,0,3	Enable read mode in the 8828D with an F(17) A(0) N(3).
TALK	Execute CAMAC cycle by addressing 8901A to Talk.

Read Data

OUT 2,0,3	Send F(2) A(0) N(3) to 8828D – command to read data.
IN B1,B2,R	Read two words to determine location of first sample.
IN B1,B2,R	
OUT 106	Set 8901A up for a high speed block read of 16-bit data words.
IN B1,...Bn,R,0	Execute a CAMAC cycle and read all of the data out (at end of data, module sets Q to 0. The 8901A then sends the response byte, followed by a 0, with the GPIB EOI bit set).

Read Acquisition Parameters

OUT 98	Program the 8901A for a 16-bit data word.
OUT 0,0,3	Send F(0) A(0) N(3) to tell the 8828D to send its setup parameters .
IN B1,B2,R	Execute CAMAC cycle and get 2 bytes containing its acquisition parameters and the CAMAC response byte.
OUT 1,0,3	Send F(1) A(0) N(3) to latch the 8828D offset value into a real buffer.
IN B1,B2,R	Read the 8828D input offset.

6010 Guide

Using ASCII control commands rather than decimal words, the 6010 controller provides the same functions for the 8828D Series as the 8901A. An 8828D control subroutine using the 6010 is shown below ("#" indicates a comment).

```
    integer *2 crate      # GPIB Address of Crate
    integer *4 LAM        # LAM Station
    integer *2 NEW DATA[8192]
# assume 8828D in slot 3
# User-written subroutines:
# CCRATE (GPIB ADDR) – sets GPIB address for following
# GREAD & GWRITE calls.
# GREAD (var, count) – reads bytes into variable from GPIB
# GWRITE (string) – writes command string to GPIB
# RDSTB – read status byte (to clear it out of the 6010)

Call CCRATE (ADDR) # setup GPIB address for crate
# Use F16 A0 write control word to set memory size, sampling period, and
# pretrigger to the 8828 in slot 3
    Call GWRITE ('F 16; A 0; N 3; W32772; e')

# Set offset to zero;
    Call GWRITE ('F 19; W 128; e')
# Set 6010 status byte mask in decimal:
# mask 1 = send SRQ on operation complete;
# mask 5 = only look at LAM when operation done.
    Call GWRITE ('MASK 1, 80; MASK 5, 6')
# Enable LAM on 8828D and arm
    Call GWRITE ('F 26; e; F 9; e')

# Loop waiting for SRQ
# This is the routine to execute when SRQ is detected.
# SPE, read status byte, SPD
    Call RDSTB
# Set block format off, 16-bit read, binary representation; blocksize of 8192; tell
# 6010 to read 16-bit word from CAMAC
    Call GWRITE ('CFMT OFF, WORD, BIN; CBLS 8192; CAMAC_WIDTH 2')
# clear LAM, set pointer to beginning of memory, read data
    Call GWRITE ('F 10; e; F 17; e; F 2; e, RB')
# read 8192 samples into buffer called NEWDATA.
    Call GREAD (NEWDATA, 8192)
```

Burst Mode

The 8828D operates in either Normal Mode or Burst Mode. In Normal Mode, the minimum physical memory size is 32K bytes and the maximum size is 2 megabytes. Active memory is a portion of physical memory defined by the user in multiples of 16K bytes. Memory cannot be read out until all of the active memory has been filled with data.

In Normal Mode, contiguous waveform samples collected at the selected sampling rate are loaded into consecutive memory addresses. Pretrigger sampling is available from 0/8 to 8/8 of active memory. The duration of the digitized waveform depends on sampling rate and total memory employed.

In Burst Mode, the 8828D records only during the presence of a burst control signal. The user can record signals of interest and avoid recording during deadtime. Burst Mode allows efficient use of memory when digitizing many short record segments back to back. Burst Mode records only post-trigger data; pre-trigger acquisition is only possible via external delay times. It is described in Figure 20 and LeCroy Application Note 2014.

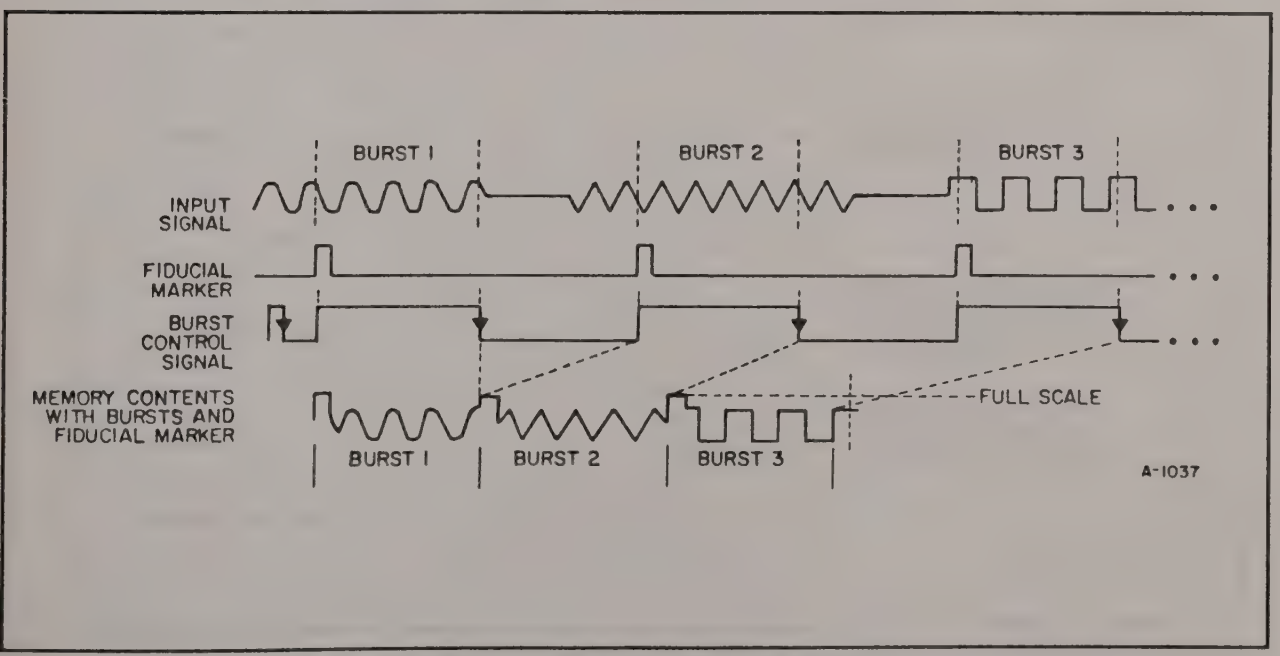


Figure 20: Burst Mode

Burst mode is selected by jumper on the side panel of the instrument. In this mode, the front-panel Stop Trigger Input is used as a clock control. Data will be transferred to memory only during valid/invalid (user-selectable) trigger conditions. The user selects the trigger slope which stops data transfers into memory (via side-panel jumpers) .

When the clock is asynchronous to the burst stop signal, the length of the acquired burst may vary by a few samples. To ensure proper registration, it is recommended that a time reference pulse be injected into the High Level Input at the beginning of each segment in order to identify each segment when reconstructing the data from memory. This reference signal is called a fiducial marker.

Pretrigger sampling must be set to 0/8 when using the burst mode.

Note that the first 16 waveform samples belonging to the first burst are not valid data. Similarly, the last 16 samples belonging to the last burst must be discarded. However, all of the remaining waveform samples contained in all other bursts are valid.

Model 2323A Burst Generation

Burst gate signals can be generated by LeCroy modular gate and delay generators Models 2323A and 4222. The 2323A provides manual or programmable dual channel variable gate functions. It has 50 nsec timing resolution and thus is not ideal for high-accuracy 8828D Burst Mode recording.

For trigger burst operation (Figure 21), follow the instructions in the 2323A manual to set the output levels to TTL. To arm the 8828D in Burst Mode, set Channel A gate to 50 nsec. This gate signal must be sent to the 8828D STOP input to arm the system before gating in "burst" segments. Use the Channel B gate to set to the desired length of the burst. Combine the Channel A NIM output and Channel B NIM output using 50 Ω cables and a power splitter. Cable the output of the splitter to the 8828D STOP Trigger connector. The trigger applied to Channel B start input initiates the burst. Set Channel B Delay to 50 nsec (DEL is set for TTL on the 2323A side panel) to provide a fiducial marker at the High Level Input of the 8828D. The following timing diagram shows the sequence.

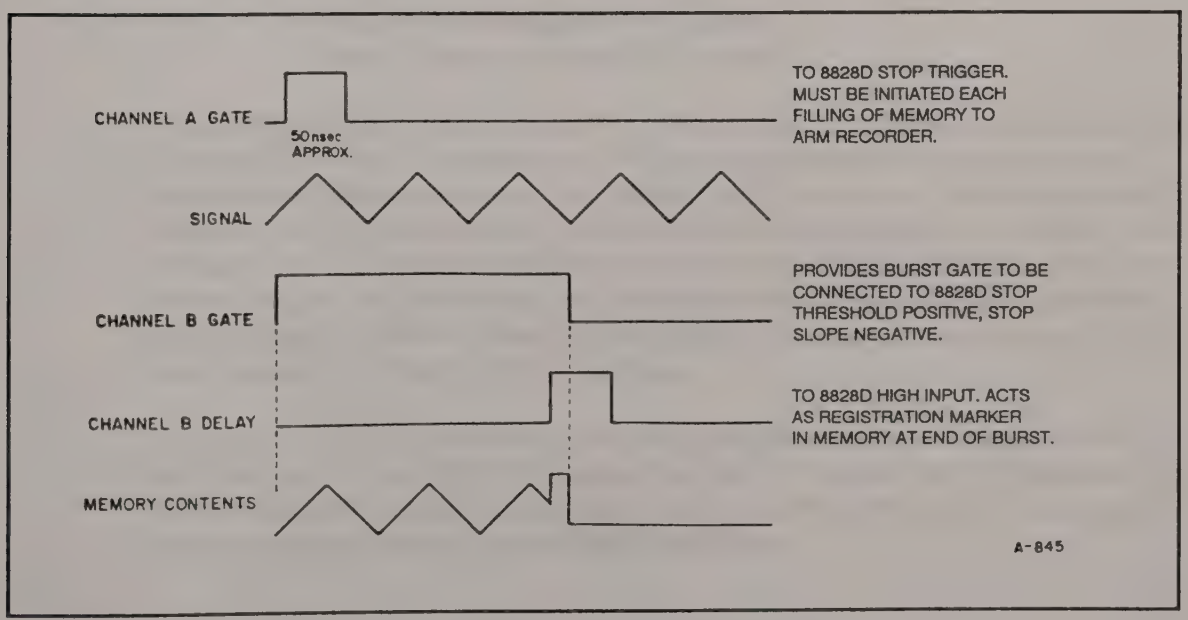


Figure 21: 2323A as Burst Generator

For delayed trigger burst operation (Figure 22), feed the system trigger to START on Channel A, which initiates the trigger delay duration. Take the NIM out signal from Channel A into the Channel B START. Note that depending on the polarity set for the output levels, the 2323 start threshold will require adjustment to ensure proper triggering of the unit. Set the gate of Channel B to equal the desired Burst recording time.

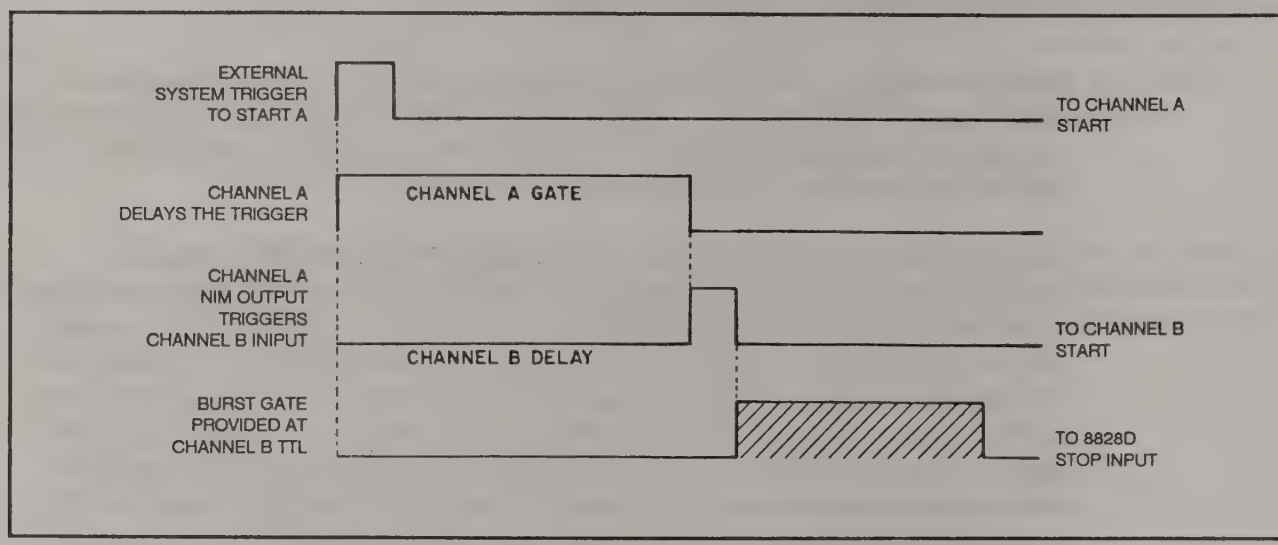


Figure 22: 2323A Delayed Trigger Burst Operation

Model 4222 Burst Generation

The 4222 provides a programmable gate suitable for 8828D Burst Mode operation. It has 1 nsec timing resolution. Both WAVEFORM-CATALYST software and 6920-DL Driver Library support the 4222. If you prefer CAMAC programming, see the 4222 manual for details.

Set the side panel of the 4222 to RETRIGGER ENABLE, GATE ON for channels 1, 2, 3, 4, and set the slope of the system start signal. Connect the system trigger to TRIG IN on the 4222. The unused TRIG IN connection should be terminated with 50 Ω. The 4222 trigger level is front-panel manually adjustable from -1.5 V to 1.5 V.

The 4222 gate time determines the 8828D burst recording time. Programmable 4222 delay times determine the burst start and stop times with respect to a trigger time. The programmable delays on channels 1 through 4 are set as follows:

Gate 1	Delay 1: Rising edge of GATE pulse 1 (beginning of burst recording)
	Delay 2: Falling edge of GATE pulse 1 (end of burst recording)
Gate 2	Delay 3: Rising edge of GATE pulse 2
	Delay 4: Falling edge of GATE pulse 2

The duration of each gate is delay 2 (4) minus delay 1 (3). Gates 1 and 2 are available from OUT 1 and 3 respectively. The two gates provide completely independent burst gate sources for two different 8828D modules. For a single 8828D, connect the 4222 inverted OUT 1 to the STOP TRIGGER input of the 8828D. Refer to Figure 25 for a timing diagram and example. NOTE: The 4222 will not accept another trigger until the longest programmed delay expires. For a fiducial timing mark indicating where two burst of data adjoin in memory, connect the 4222 P2 pulse output to the 8828D High Level Input.

The 1 nsec resolution of the 4222 and excellent jitter allow precise placement of the burst gate in reference to the system trigger. By synchronizing the system trigger to the 8828D digitizing clock the burst gate width can be tuned to repeatedly provide the same number of samples in each burst.

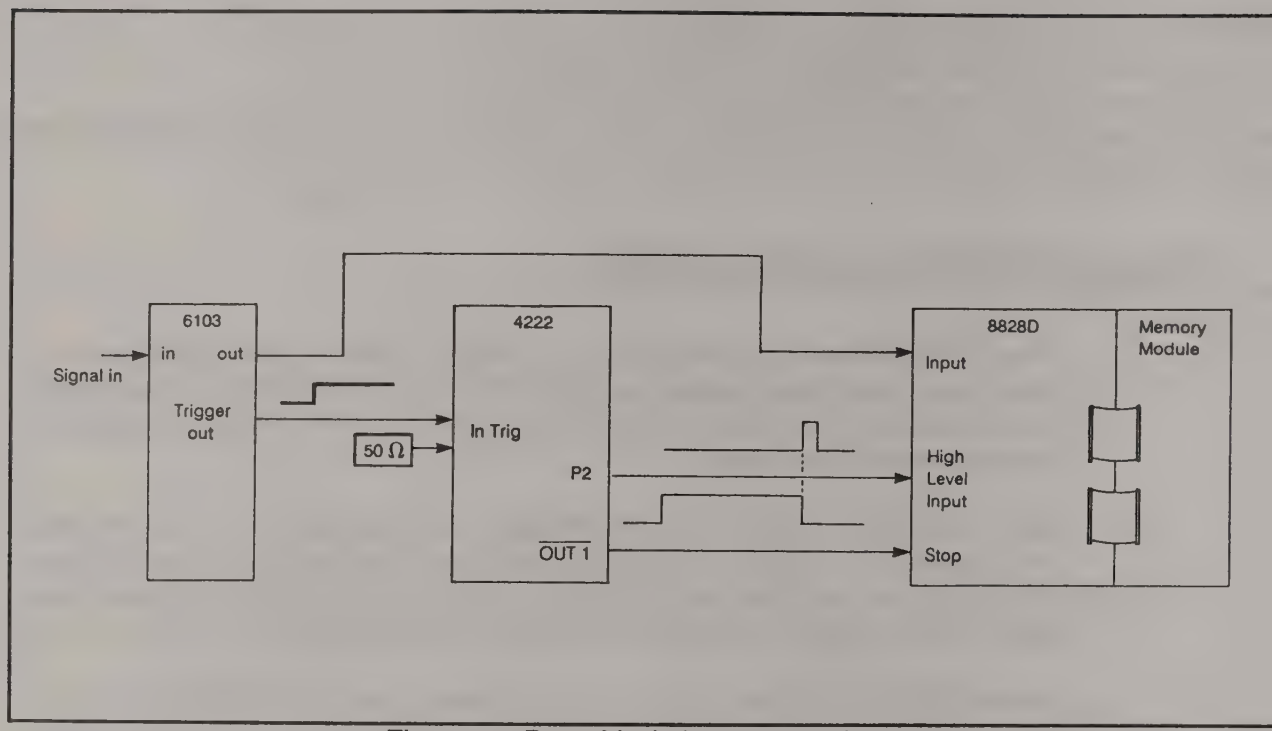


Figure 23: Burst Mode Interconnections

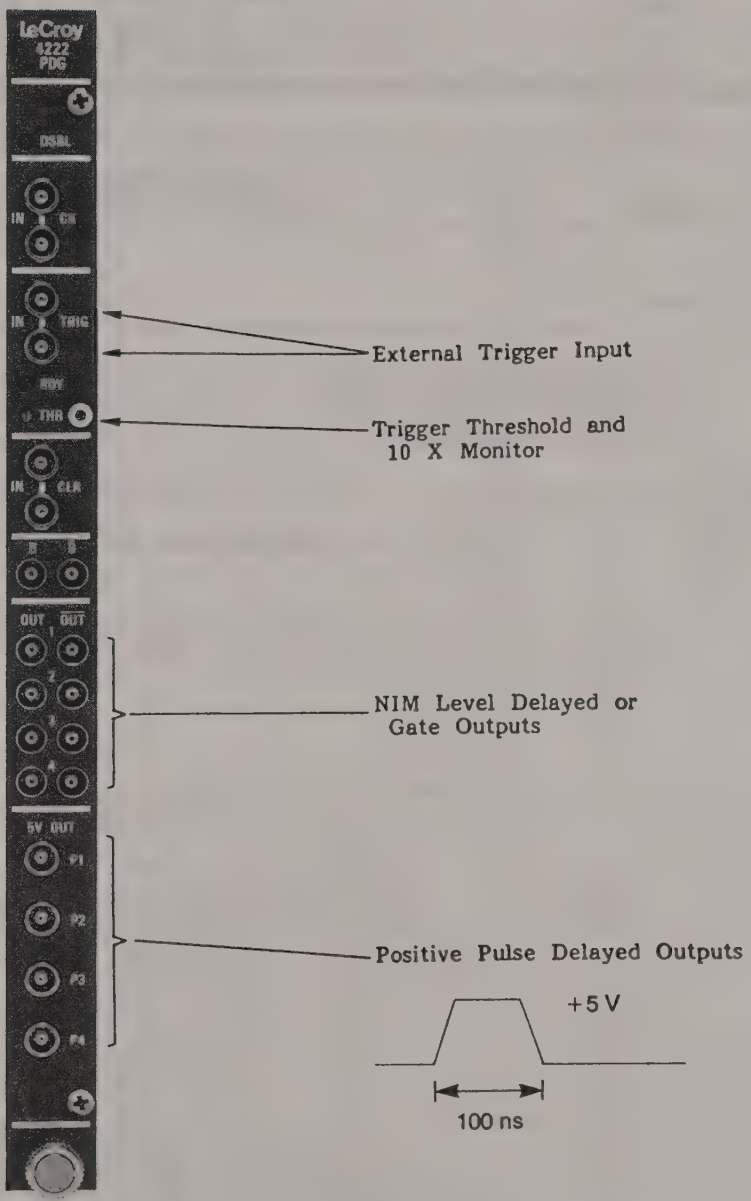


Figure 24: 4222 Front Panel Description

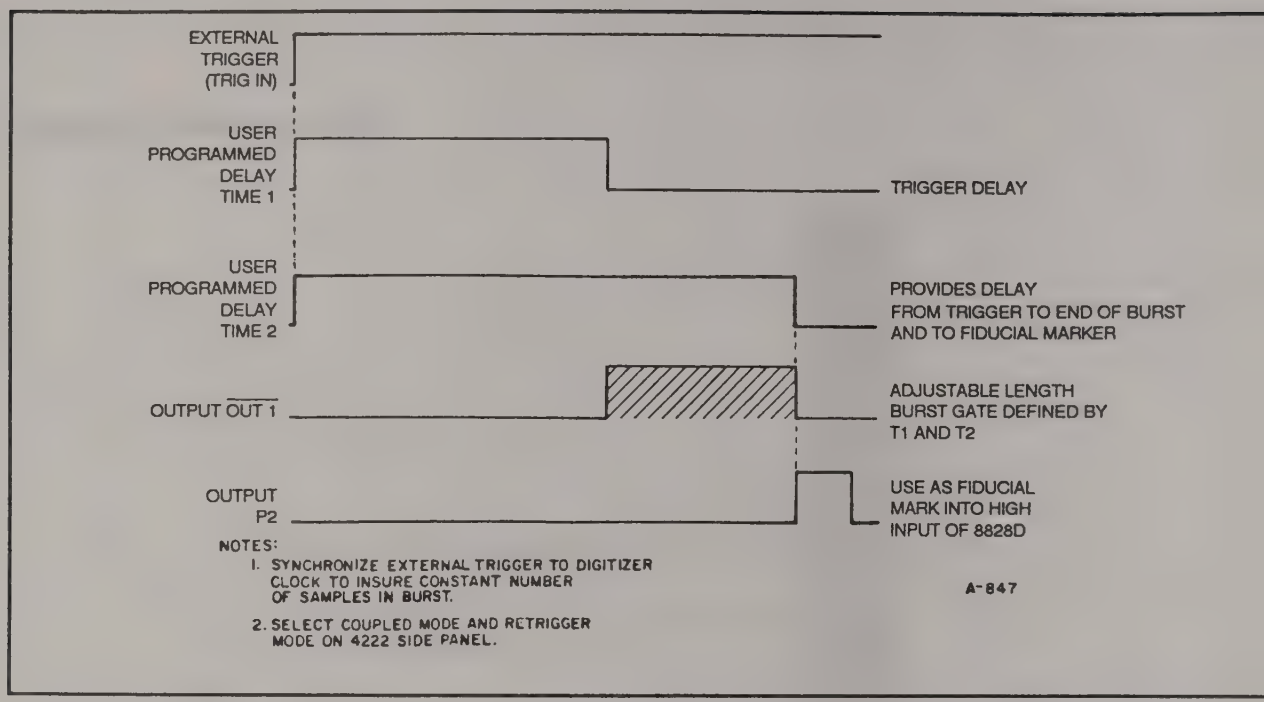


Figure 25: 4222 Delayed Burst with Fiducial

THEORY OF OPERATION

Figure 26: System Block Diagram

ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) resides on the left hand circuit board and communicates with the Controller via an internal cable. It transmits data to memory via the front-panel data bus. Critical high-speed analog processing components are all contained in state-of-the-art thick-film hybrid circuits.

In the following description WXX-Y means device W number XX on board Y where Y is R (righthand board) or L (lefthand board). The 8828D-1 is the lefthand board and the 8828D-2 is the righthand board.

Analog Processing

Refer to the ADC block diagram. Signal inputs are routed via overload protection diodes to U1-L, the input amplifier. This provides a gain of 5 from the Input and 0.5 from the High Level Input to its output. Also the offset voltage provided by the DAC (U7-R) on the controller card is summed with the input signals. Q3 provides bias current for the output stage of U1-L.

U1-L output is routed to the input of U2-L. U2 is an 8-bit flash ADC. Full scale signal input to U2-L is ± 0.64 V, corresponding to $\pm$ 1.28 V at U1-L output. Adjustable reference voltages for U2-L ADC are provided by U5-L and R59-L. Since U1 is an inverting amplifier, the flash ADC output data are inverted with respect to the input signal. U3 and U4 re-invert the flash output.

Digital Processing

The digital process probides to basic functions: clock generation and selection and byte stacking. Some sections of the controller circuits reside on the ADC circuit board; this avoids the transmission of clocks and data between ADC and controller at greater than 50 MHz.

The internal clock consists of U41-L, a 200 MHz crystal oscillator with ECL output. The output is divided by U35-L and U40-L to produce the various sampling rates. U37-L, U38-L, and U39-L decode the control signals F4, F5, and F6, which are transmitted via the internal cable from the controller card to select the desired sampling rate or external clock.

U31-L selects between internal and external clock. When external clock is selected, VR9-L shuts off power to the crystal oscillator, thus eliminating the possibility of coupling between the internal and external clocks.

U32-L and U33-L buffer and fan out the clock. A high-quality twistedpair cable carries the clock to the differential inputs of the flash ADC. An additional high-quality twisted-pair cable and differential receivers U30-L delay the clock and carry it to the trigger circuitry and U33. This gate fans out the delayed clock to the address counter (U26-L), the post-trigger counter (U27-L), and the byte stackers (U12-L, U13-L, U14-L, U16-L). The counters are split between the ADC card and the controller card, thus scaling the 200 MHz sampling clock down to 50 MHz before it is transmitted to the controller card via the internal cable. AD1 clocks the address counters and PT1 clocks the post-trigger counters on the controller card.

The scalers U26-L and U27-L operate only when the system is writing to memory. When not writing to memory, the data generated by the ADC is ignored. When U24-L and U21-L are set to start the scaling of the address counter, the clock to the byte stacker latch (U6-L, U7-L, U8-L, U9-L, U10-L) begins transmitting data via the 50-conductor cable to the memories. The byte stacker latch accumulates 4 bytes before transmitting them to the memory.

When a stop command is received, either via the front-panel connector and stop comparator (U22-L) or the CAMAC function code F(25) and A(0) as decoded by the controller board, the flip flop U18-L is clocked which then enables the post-trigger counter and the clock to the controller card PT1. When the post-trigger samples have been taken, the two LSB's of the address counter are latched by U20-L and saved on the controller card as the start address. Also at this time the write signal to the controller is negated. The address counter and post-trigger counter scalers are then reset and disabled until the next sampling command, F(9) and A(0), is received by the controller.

DIGITAL CONTROLLER

The controller portion of the 8828D resides on the righthand board and communicates with the ADC board through a 20-conductor cable connecting the two. The controller board is called the 8828D-2 board. Logic consisting of ECL, CMOS, and TTL is used to minimize power dissipation and maximize performance. ECL is used in the address counter, post-trigger counter, and fast control logic. Registers that are backed up by batteries are CMOS. The rest of the logic is low power Schottky TTL.

CAMAC Control

A(0), N, and NOT F4 are decoded by U60-R. U80-R uses the output of U60-R and the remaining F lines to decode the commands accepted by the 8828D Series. An X and Q response is generated for all commands by U71-R. Since most commands generate these responses, X and Q are inhibited by those commands that require X = 0 and Q = 0. Q is inhibited by the inputs to U82-R. X is inhibited by the inputs to U71-R.

Commands that latch data do so at the time of S1. These commands are AND'd with S1 to produce the appropriate strobes. S2 is used to increment the address counter when reading data so it is AND'd with F(2). F(17) and S2 loads the starting address of the data into the address counter, sets the valid data flip flop, and sets the first byte flip flop. F(9) and S2 set the TR8828D Series into the digitizing or ready state. F(25) and S2 start the post-trigger counter by enabling PT1 on the 8828D-1 board.

Read commands enable open collector drivers onto the CAMAC read lines. All the registers that can be read by CAMAC must have their signals translated to TTL levels. Low power comparators (LM339s) are used as translators.

Write data from CAMAC is translated to the control registers with LM339 comparators. The registers use -0.8 V and -5.2 V for power with VDD at -0.8 V and VSS at -5.2 V. CMOS can drive ECL logic directly if these supplies are used.

Memory Control

Figure 27 is a block diagram of the logic that controls the addressing of memory. The memory is organized as a circular file of data samples. There are two operating modes for the memory control, write to memory and read memory.

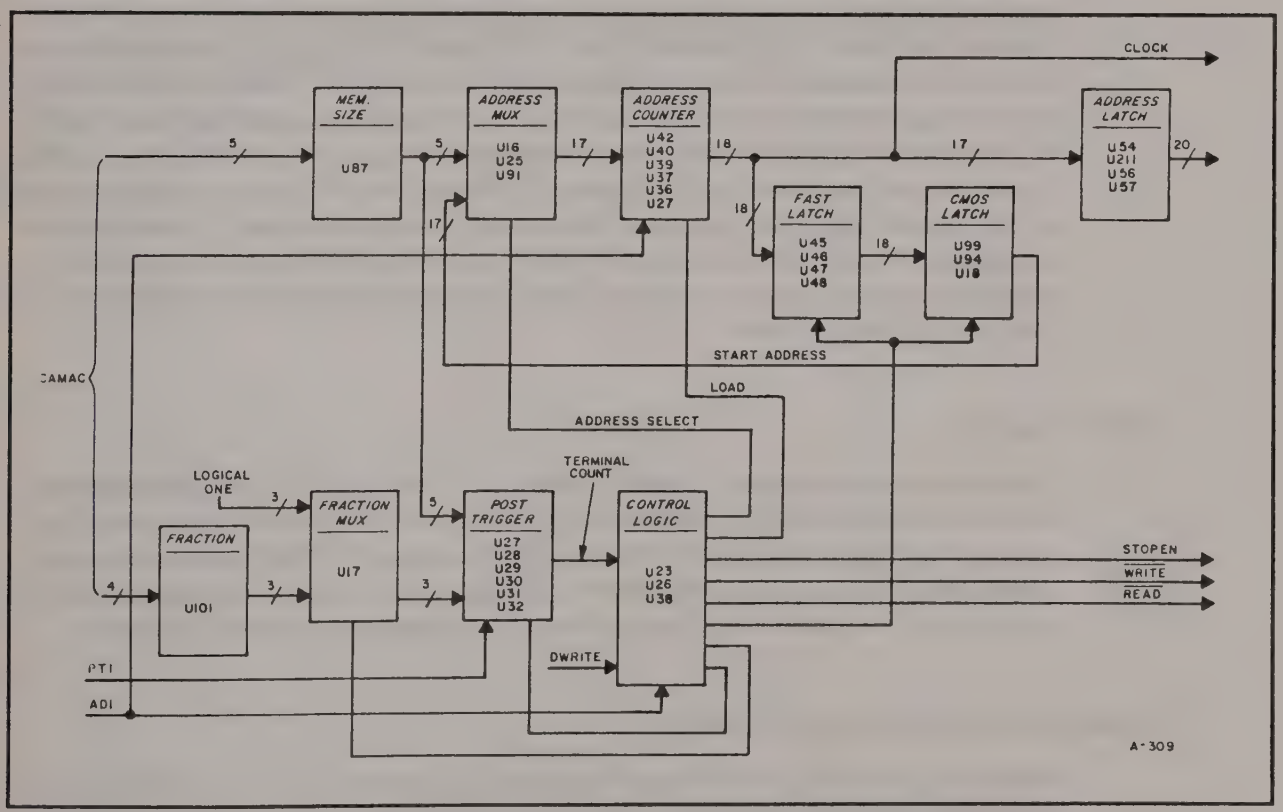


Figure 27: Controller Block Diagram

Write to memory is initiated by F(9) and A(0). The flip flops U18-L, U21-L are set to wait for the Stop. The flip flops U24-L U21-L are set to start the scaling of the address counter and to generate a write to the memory. During the Write mode the 1's complement of the memory size is multiplexed to the data inputs of the address counters. The address counter counts up to terminal count, reloads the 1's complement of the memory size, and proceeds to count up again. Therefore, memory is loaded with data at addresses starting at full scale minus memory size up to an address of full scale minus 1. This cycle is repeated until a Stop is received.

Stop starts the post-trigger counter. When the write to memory is initiated, F(9) and A(0) loads the post-trigger counter with the 1's complement of the memory size and the fraction or pretrigger size. The post-trigger counter is two counters in series. One (U27-L, U28-R, U29-R, U30-R, U31-R) counts up to the memory size divided by 16 repetitively and the second (U32-R) counts to the fraction multiplied by 16 once. The overall effect is to count the post-trigger samples. At the terminal count of the post-trigger counter, Write is negated. In addition, not Write sets the internal LAM flip flop U95-R. The data can now be read from memory.

Asserting F(17) and A(0) loads the starting address from the CMOS latch into the address counter and loads the memory size and zero pretrigger into the post-trigger counter. Valid Data flip flop U95-R and First Byte flip flop U96-R are also set. The first assertion of F(2) and A(0) will put B0 and B20 onto the R1 and R2 lines of the CAMAC dataway. This is the status word, indicating the position of the start byte in the 2-byte words that are read from memory. The second and successive F(2)s increment the address counter and the post-trigger counter by two. Scaling by two occurs because both flip flops in U27-R are enabled, which enables clocks to the second bit of both counters. The memory modules places 2 bytes onto the read lines of the CAMAC dataway for every read clock. When terminal count is reached in the post-trigger counter, Valid Data is negated and further F(2)s will generate a Q = 0 response.

ADC Control

Offset is supplied to the ADC via connector J4. An 8-bit DAC (U7-R) produces a current which flows through a resistor (R17-R) and a potentiometer (R13-R). The resultant voltage is buffered by U5-R. A CMOS register (U78-R) stores the offset value when F(19) and A(0) are asserted. Asserting F(1) and A(0) will enable the stored word via U79-R onto the R9 through R16 lines of the CAMAC dataway.

Power Fail and Battery Backup

Power failure in the controller card is detected by monitoring three of the power supplies used by the card. Zener diodes, resistors, and an opto isolator detect the presences of the ±24 V supplies. A series string of resistors and LED's check the -6 V supply. The result of these checks are AND'd together to produce POWERON. SPF from the ADC and memories is trans lated and AND'd with POWERON to enable the X response. Failure of any supply will disable the X response.

Battery backup is accomplished with battery B1-R and diode CR3-R. Resistor R4-R is used to monitor current when the power is off. When a power fail is detected all register clock inputs are held high and tri-state outputs are disabled. Capacitors C6-R, C134-R, and C146-R maintain the logic supplies at their nominal levels while the power fail logic turns everything off.

The -2 V supply is distributed between two regulators and fanned out to the 100 Ω pull-downs.

MEMORY MODULES

Refer to Figure 28 for a block diagram of the memory design.

Memory modules contain sixteen 2K x 8 CMOS static RAM IC's, sixteen 8K x 8 CMOS static RAM IC's for MM8105, or sixteen 32K x 8 CMOS static RAM IC's for MM8106. Read and write cycle time for these IC's is 120 nsec in MM8103A, MM8105, and MM8106, 70 nsec in MM8104. At the maximum data rate 4 bytes appear at the front panel every 40nsec. These 4 bytes are assembled into an 8-byte word which is presented simultaneously to an upper bank of eight memory IC's and a lower bank of eight memory IC's. Only one bank gets a write pulse for each 8-byte word. Thus, the worst case minimum cycle time is 160 nsec in MM8103A, MM8105, and MM8106, 80 nsec in MM8104, much slower than the cycle time of the memory IC's.

CAUTION: Unsolder one lead of the battery or remove jumper E1-E2 before attempting repairs on this unit.

Write Cycle

Address and data lines are terminated with removable 100 Ω SIP resistors. The differential clock line is terminated with a single 100 W removable resistor. Of the 20 address lines received by the memory the upper six address lines are used as module select lines. These six lines are compared with the front-panel switches to determine whether the module is selected. Exclusive OR's perform this function, generating the signal called SEL which enables appropriate gates in the module.

Both the upper bank and lower bank see their addresses and data inputs from similar sources. This ensures symmetric operation with respect to the address and databus. Address and data latches for both banks accomplish this symmetric operation. Figure 29 shows the timing of address, data, and write enable at each memory bank. The data is common to both banks, strobed only at the appropriate time.

Once a write cycle has started, the cycle is completed independent of the state of the SEL line. This is important when more than one module is in a system. As the address bus deselects one module and selects another, the previous write cycle to the last bank must be completed. Write cycles overlap from one module to the next because of pipelining of data within the modules.

Flip flops in 1H control the timing of the write enable pulses to the memory IC's. Clocks are delayed appropriately with gates in 1K. Note that signals UBDI and LBDI are not enabled by SEL. This ensures a full-width write enable as long as the clock and address lines continue to toggle.

Read Cycle

During the read cycle AB1, AB2, and AB3 are decoded to read 2 bytes at a time from the 16 memory IC's. Open collector drivers put the bytes onto the R1 through R16 read lines of the CAMAC dataway.

The Read line is simply the decoded F(2) and A(0) from the waveform recorder. The address changes near the end of the CAMAC cycle when S2 increments the address in the waveform recorder. This address change before the end of the Read cycle will create a short enable pulse from the decoders.

Power Fail and Battery Backup

The two power supplies are sensed with a series string of diodes and a resistor. As long as ± 5.2 V is available, the red LED will be enabled and SPF will be low. Loss of power will turn off the red LED and pull SPF to -.08 V. SPF is driven by an open emitter and must have a pull-down in the waveform recorder. On power fail the battery maintains the data in the CMOS memories. Chip select is held high when power is off. Pull-downs to ground on the address lines keep the current requirements of the memory IC's to a minimum during power fail. Resistor R12, in series with the battery, is used to measure the current drain from the battery when the power is off. When the battery is installed, the current is measured to ensure a typical five-year lifetime of the battery.

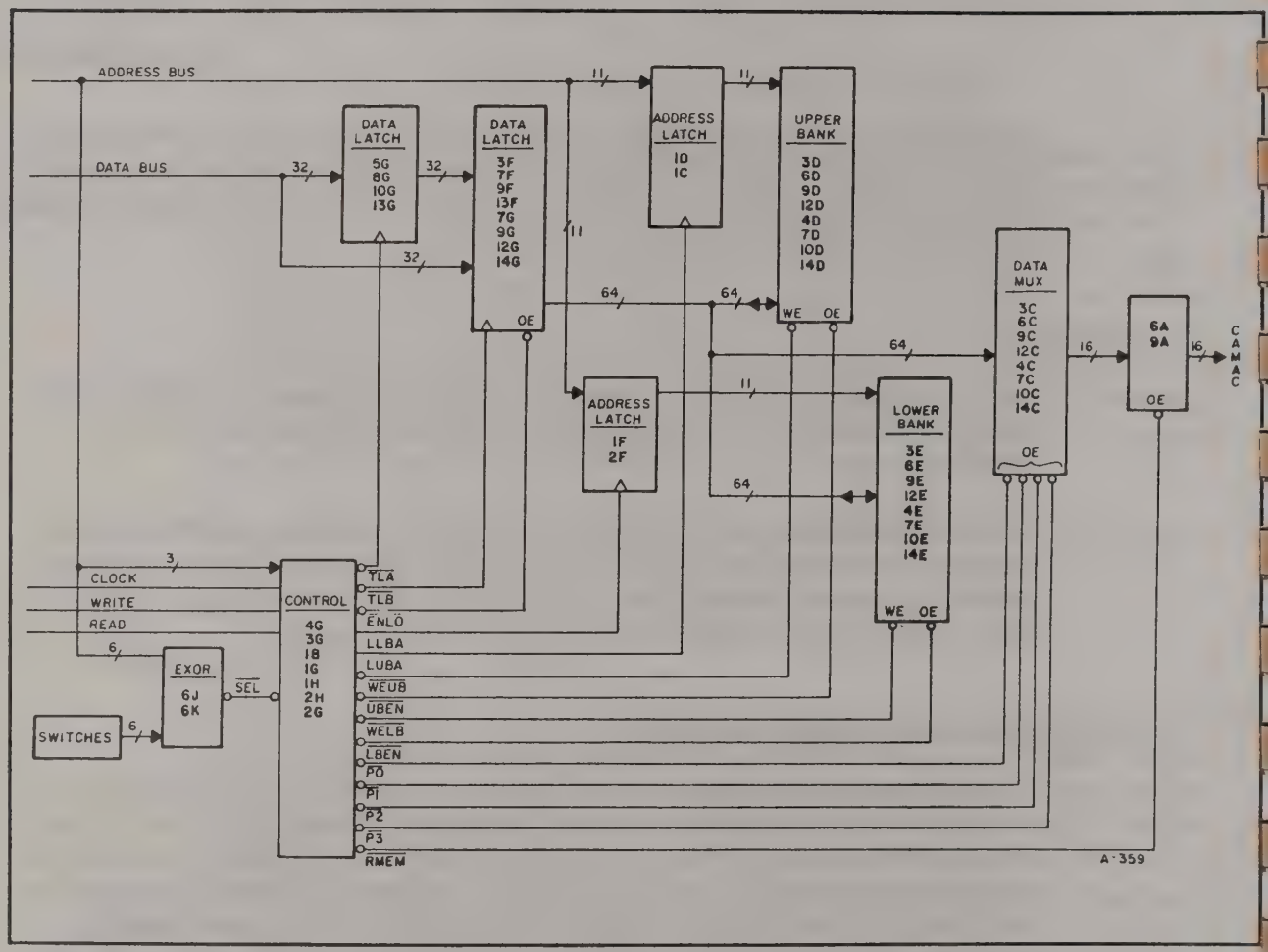


Figure 28: Memory Design Block Diagram

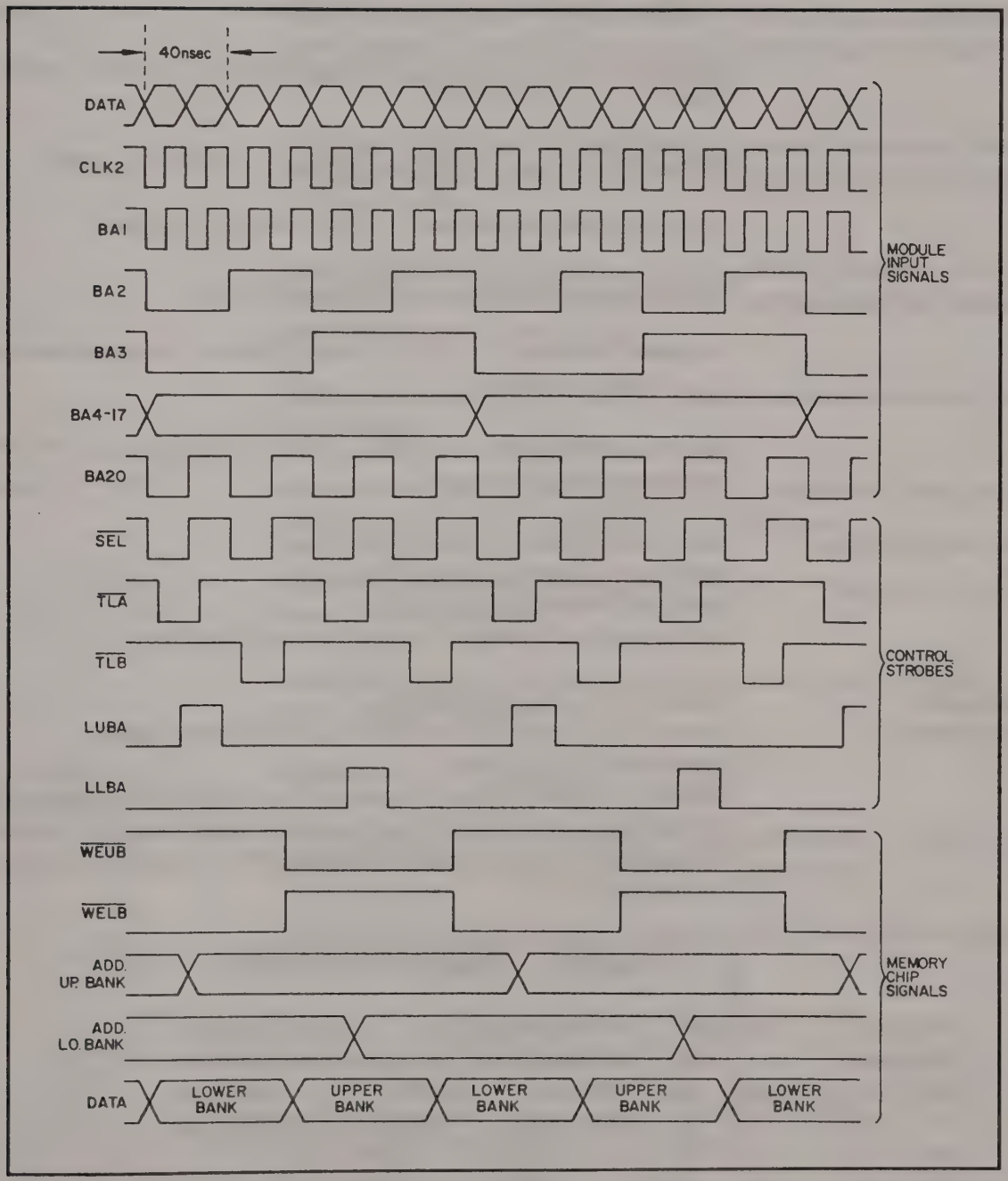


Figure 29: Timing of Address, Data, and Write Enable at each Memory Bank

SPECIFICATIONS

Signal Input

Amplitude Range: 510 mV peak-to-peak.

Impedance: 50 Ω +3% DC; <7% reflection from 3 nsec edge; VSWR of <1.15 at 100 MHz.

Bandwidth: DC to >100 MHz (-3 dB), to >50 MHz (-1 dB).

Offset: Programmable over ±1/2 full scale in 256 steps.

Temperature Stability: ±1/2 mV/°C maximum.

Overload Recovery: ±1% in 25 nsec from a 1.5x overdrive pulse of <1μsec duration.

Overload Protection: ±2.5VDC; ±500 V for 30nsec or ±100 V for 100 nsec with 50 Ωsource.

High Level (X10) Signal Input

All characteristics same as above except
Amplitude Range: 5.1 V peak-to-peak.
Overload Protection: ±7.5VDC.
Configuration: Internally summed with normal input.

Stop Trigger Characteristics

Slope: + or – set at side panel.
Level: ±2 V, adjusted and monitored from front panel.
Impedance: 50 Ω source.
Modes: In Normal Mode, trigger switches from pretrigger to post-trigger sampling; digitizing stops when post-trigger sampling complete. In Burst Mode clock is disabled whenever the trigger level is below the preset value.

Model	Storage/Unit	Speed
MM8103A	32K	100 MB/sec
MM8104	32K	200 MB/sec
MM8105	128K	100 MB/sec
MM8106	512K	100 MB/sec

Memory

Active Memory Size: Programmable in 16K sample increments up to the total size of memory installed (2M samples maximum if using MM8105/MM8106 memory modules).

Pretrigger: Memory can be divided into pre and post-trigger sample storage, programmable from 0/8 through 8/8 in increments of eighths of active memory.

Burst Mode: Side-panel jumper option enables front-panel Stop Trigger Input to double as a clock control. (Pretrigger and programmed stop features can not be used).

Battery Backup: Data in memory is preserved when external power is removed.

Timebase

Internal: 200 MHz 0.01% crystal oscillator and divider provide sampling periods of 5, 10, 20, 40, 80, 160, or 320 nsec.

External: User clock can be supplied via 50 Ω front-panel connector; ≤200 MHz ECL.

Clock Out: ECL level signal available via front-panel connector; period equal to sampling rate.

Analog to Digital Characteristics

Resolution: 8-bit binary word (2 mV/LSB.)

DC Accuracy: Errors are less than ±1.5 LSB's plus 1/2 LSB quantizing error from best linear fit over entire range.

AC Accuracy: A reconstructed digitized pure sine wave has a minimum dynamic accuracy as follows:

Signal Frequency	Signal Amplitude	Effective Bits		Sig/Noise Ratio(dB)	
		min	typical	min	typical
To 5 MHz	80%	6.8	7.3	40	46
20 MHz	80%	6.3	7.0	37	43
50 MHz	50%	6.0	6.4	33	39
100 MHz	50%	5.5	5.9	29	37

Aperture Uncertainty: ±5 psec maximum.

Noise: RMS noise < 1.7 counts, not including misconversions. The probability of a misconversion (defined as > 3 counts) is typically less than one per million averaged over the entire amplitude range.

General

Connectors: All front-panel connectors are BNC, except FAST DAC, ARM BUSY, TRIG BUSY, and CDS (manual control enable) which are Lemo. Cables with either BNC or Lemo connectors are available from LeCroy.

Status Lights: Front-panel LED's indicate power and digitizing status.

Module ID: 8-bit side panel switch allows a unique user assigned module identification number which can be read to the dataway.

Power Requirements:

	+6 V	-6	24 V	-24 V
8828D	0.775 A	6 A	220 mA	175 mA
MM8103A	2.9 A	1.8 A	-	-
MM8104	2.9 A	1.8 A	-	-
MM8105	2.9 A	1.8 A	-	-
MM8106	2.9 A	2.1 A	-	-

Internal Battery: Replaceable Lithium battery (lifetime > 2 years) in each memory module and digitizer automatically becomes power source for memory and control registers.

Environment: Proper operation requires +15°C to +25°C intake air with sufficient flow to maintain temperature rise of exhaust air to < 15°C (+30°C intake air allowed if sufficient airflow to maintain temperature rise of exhaust air to < 10°C), humidity up to 90% non-condensing, altitude < 10,000 ft above sea level. Storage temperature range is –10°C to +50°C.

Packaging: RF shielded module in conformance with the CAMAC (IEEE 583) Standard.

	Size	Height	Width	Depth
8828D	#3	221 mm	51 mm	292 mm
Memories	#1	221 mm	17 mm	292 mm

COMMANDS

Programming commands are listed in this section, while examples of the control sequence and a sample FORTRAN control program are contained in Chapter 2, Operating Instructions.

All CAMAC Dataway commands listed below except F(25) are disabled during conversion. To prevent possible noise induced by asynchronous digital switching, it is recommended that no unnecessary CAMAC commands be generated on the Dataway during the actual analog-to-digital conversion cycles (i.e., between arming units and receiving a Look-At-Me (LAM). The Z (Initialize) command from the CAMAC Dataway will clear and disable all LAM's and disable (unarm) the A-D converter, but will not otherwise affect control registers or stored data. All CAMAC function codes respond to A(0) only. An X- and Q-response is returned for all valid commands, except a Q-response requires that a valid data transfer has occurred (on a read or write command) or that the appropriate LAM is present (on a F(8) or F(27) command).

Parameter Setup, Status And Control Commands

Input Offset: F(1) reads from R9-R16; F(19) writes to W1-W8. Data is 8-bit binary representation of the input offset voltage where offset = 255 - N mV for N = 0 to 255.

Control Register: F(0) reads from R1-R16; F(16) writes to W1-W16. Data is 16-bit binary word, bit coded as follows:

Memory Samples (X 1024)		Sampling Period (nsec)		Pretrigger Samples (fraction of active memory)	
0	16	0	5	0	0/8
1	32	1	10	1	1/8
2	48	2	20	2	2/8
3	64	3	40	3	3/8
4	80	4	80	4	4/8
5	96	5	160	5	5/8
.	.	6	320	6	6/8
.	.	7	EXT	7	7/8
.	.			8	8/8
127	2048				

W/R8 is not used; W/R16 is available to the user for storing programmable identification flag bit or event related information. Writing or reading it does not affect any other module parameter.

Trigger Arm: F(9) will arm the unit, and if the internal clock is used, starts digitizing, allowing the next trigger to initiate digitizing stop cycle. If the external clock is selected, F(9) will enable the clock input, but then requires an external clock to digitize and respond to a Trigger of F(25). All other commands are disabled when in the armed state.

Internal Trigger: F(25) generates an internal trigger (OR'd with external trigger input). Used in auto trigger modes or when calibrating, testing or demonstrating and no external trigger is available.

Module ID Word: F(3) reads an 8-bit binary value set on R1-R8 from switch located on bottom of module.

Memory Access Commands

Enable Read Mode: F(17) sets address counter to beginning of data record. Must be followed by F(2) or Z.

Read Data: F(2) reads two 8-bit samples on R1-R16 from the current memory location, then increments memory address by one. The two 8-bit samples contained in each 16-bit word are in binary representation, lower byte first. The first byte is the time vernier, see below. The next 15 bytes and the last 16 bytes may be inaccurate and therefore should be discarded. Read must be preceded by F(17) command (Enable Read Mode) to set address counter to beginning of data record. Q = 1 while memory data is valid, going to 0 after last data word.

Trigger Time Vernier: The high-speed nature of the digitizer requires that four samples be simultaneously transferred to memory. R1 and R2 of first byte specifies which of the four bytes (of the next two words) starts the data record as follows:

R1-R2	First Sample
0	R1-R8 of 1st word
1	R9-R16 of 1st word
2	R1-R8 of 2nd word
3	R9-R16 of 2nd word

Note that even though this defines the location of the first sample, the actual data may be inaccurate until the 17th sample (9th word) is read.

LAM Commands

The LAM line on the CAMAC dataway indicates that a stop trigger has occurred and all post-trigger samples have been stored in memory.

Test LAM Status: The status of LAM also can be checked by F(8) or F(27) where a Q = 1 response indicates that LAM is present. F(8) requires that LAM Enable be set.

Enable LAM: F(26) will allow a LAM to drive CAMAC dataway LAM line.

Disable LAM: F(24) will not allow a LAM to drive CAMAC dataway LAM Line. Z or C will disable both LAM's.

Clear LAM: F(10) will clear LAM.

CONTROLS AND CONNECTORS

Front Panel

Pwr/N: This dual LED flashes green when CAMAC N is asserted. Red indicates all power supply voltages are present on the control board of the module.

L/Rdy: This dual LED flashes green when the sampling clock has been enabled ready and the unit is digitizing and storing data. When red, it indicates that the digitizing sequence is completed and that internal LAM is set.

Pwr (Memory Module): This dual LED flashes green when the memory is being accessed. When red, it indicates that power is present.

Input: The analog input accepts 510mV p-p signals with a DC offset in the range of ±1/2 full scale.

High Level Input: This input is similar to the Input described above except the input range is 5.1 V p-p. All other parameters remain the same.

Clock-In: This input is an ECL input terminated in 51Ω . Data conversion is initiated by the positive edge, accepting an input frequency of ≤200 MHz with a 50% duty cycle. The input is protected against 5 A transients for 1msec. The clock must last 16 cycles after the last data sample so that the transfer to memory of the last 8 data bytes is completed. At the users option the 51 Ω resistor can be terminated to ground or -2 V. The unit is shipped with the ground connection.

Clock-Out: This output provides an ECL compatible output of the internal or external sampling clock. At the users option the ECL output may be pulled down to -5 V with a 110 Ω resistor. If no pulldown is selected, the output must be terminated externally with 50 Ω to -2 V. If the internal pulldown is selected, the output will drive 50 Ω to ground.

Stop: This input stops acquisition after the selected number of post-trigger samples has been stored. The minimum pulse duration is 8 nsec. The input is protected against 5 A transients for 1 msec. The threshold can be set and monitored from the front panel. The threshold range is ±2 V. Side-panel adjustments allow ±slope triggering and 51 Ω termination to ground or -2 V.

CDS: A low-level input forces the equivalent of a CAMAC N, which can be used to identify the digitizing module to the instrument controller. This input accepts TTL level signals and is pulled up to +5 V with 1 kΩ.

Fast DAC: This output provides the reconstructed input signal. This output is generated from data samples before they are stored in memory. This data appears at the selected sampling rate. The full scale range is approximately 1 V. The Fast DAC output requires a 50 Ω termination to ground.

Arm Busy: This output is TTL open collector output indicating the unit is sampling and is ready for a Stop Trigger. A side-panel jumper allows selection of the polarity of this signal.

Trig Busy: This output is a TTL open collector output indicating that the unit has accepted an internal or external trigger and is acquiring the post-trigger samples. A side-panel jumper allows selection of the polarity.

Address: This 34-pin connector contains the address signals and control lines for writing to or reading from the memories. The signals are single-ended ECL except for the clock, which is differential. The address lines must be terminated by a memory module. The bus is unidirectional with the drivers in the 8828D Series only.

Data: This 50-pin connector contains the databus from the unit to the memory modules. The databus is 4 bytes wide, ECL, and must be terminated by a memory module. This bus is unidirectional with the drivers in the 8828D Series only. The SPF line, indicating power-fail in the memory modules, is on this connector.

Stop Thr: Multiturn potentiometer adjusts threshold level of Stop Trigger of ±2 V range. Test point provides voltage that corresponds to the level setting.

APPENDIX A: Glossary

A

Aperture uncertainty — The variation (rms) in A/D sampling period. Aperture uncertainty translates into measurement amplitude errors, especially on fast changing signals. Therefore, uncertainty should be small for accurate pulse risetime and falltime measurements.

B

Bandwidth — The useful input frequency range before internal filtering elements cause substantial signal attenuation. The 8828D's bandwidth ranges from DC to > 100 MHz (-3 dB), to > 50 MHz (-1 dB).

BFP — Blank Front Panel. Inserted in empty CAMAC slots, it ensures proper air flow and cooling of the 8828D and memory module(s).

Bipolar signal — A dynamic signal which changes between positive and negative voltage levels.

BNC connectors — Coaxial connectors used for interconnecting high frequency signals. The typical connector bandwidth is over 1 GHz.

C

CAMAC — IEEE-583 Computer Automated Measurement And Control standard. The standard defines instrument module form factor, power consumption, programming code format, a communication bus, the instrumentation mainframe (crate), and power supply levels to simplify interchangability.

CAMAC controller — A CAMAC module which controls all the instruments within a CAMAC mainframe. The controller addresses each installed instrument via dedicated lines and transfers commands and data via a common bus in the CAMAC mainframe backplane. The CAMAC controller also acts as the

CAMAC N Slot Number	The mainframe slot number pointed to by the 8828D's front-panel arrow. During bus operation, the GPIB to CAMAC interface addresses this CAMAC slot to communicate with the 8828D.
CAMAC station	See CAMAC N slot number.

D

DIP switch	A package of miniature ON/OFF toggle switches. DIP means Dual Inline Pin package for PC board mounting.

E

Engineering Change Number (ECN)	A number assigned to any LeCroy product modification for upgrade tracking purposes.
External clock	A front-panel sample-clock input for synchronizing several 8828D modules to obtain multichannel simultaneous sampling or for synchronizing one or more 8828D modules to an external frequency source.
External signal conditioning	Any type of amplifier, attenuator, transducer bias circuit, or converter which modifies the signal to match trigger or signal input characteristics of the 8828D or enables a transducer to function.

F

Full scale voltage range	The maximum voltage which the 8828D can accurately record. Two separate BNC connectors provide full scale voltage of 510 mV and 5.10 V respectively.

G

GPIB	A General Purpose Interface Bus, defined by the IEEE-488 Standard, for interconnecting instrumentation to a host computer for purposes of automation. Up to 15 instruments and controllers can be interconnected via one bus.

GPIB address	A selectable address from 0 to 31 for any instrument attached to the IEEE-488 Standard Interface Bus (GPIB).
GPIB controller	The computer which controls the activity of all instruments on the IEEE-488 Standard Interface Bus (GPIB). The controller instructs the instruments to be talkers (feed data onto the bus), listeners (accept data/commands from the bus), or inactive.

H

Harmonic distortion	Non-linear distortion of a sinusoidal input signal which causes harmonics (sines of frequencies equal to integer multiples of the input sine) to be added to the original signal. The numeric value equals the square root of the sum of the power in all the harmonic frequencies divided by the power in the fundamental, usually expressed in percentage or dBc.
Host controller	A computer with the ability to control the GPIB, store data, and execute an instrument control program.

I

IEEE-583 backplane	The CAMAC motherboard which contains the address lines and data bus. All CAMAC modules communicate digitally via the CAMAC (IEEE-583) backplane.
Input impedance	The shunt resistance, capacitance, and inductance value from the input to chassis ground in single-ended mode and from (+) input to (-) input in differential mode.
Input voltage range	See full scale voltage range.

L

LED	Light Emitting Diode, used for indicating instrument operating status.
Look-At-Me (LAM)	A digital service request made by the 8828D to the CAMAC controller via the CAMAC backplane. LeCroy 8901A and 6010 CAMAC controllers translate this signal into an SRQ digitial service request on the GPIB.

M

Mainframe	The chassis which houses one or more digitizer modules, expansion waveform memory, other instrument type modules, and the CAMAC controller.
Mainframe Controller	Either of LeCroy's Model 8901A and Model 6010 GPIB to CAMAC crate controllers. See CAMAC Controller.

N

Negative slope	The falling edge of a signal.
Non-linearity	Deviation from direct proportionality.

P

Peak-to-peak voltage	The difference between the maximum voltage and the minimum voltage of a signal within a specified time window.
Positive slope	The rising edge of a signal.
Pulse response	The digitized waveshape compared to the original pulse input which shows the linearity of gain, phase, and offset versus frequency.

R

RAM	Random Access Memory; a data storage device which allows access to any memory location without regard to the previously accessed location.
R.F. shielding	Shielding to prevent radio frequency electric fields from generating a noise voltage in signal paths.
ROM	Read Only Memory; a permanent, non-erasable, data storage device which allows extremely rapid access to data.

S

Sampling rate	The rate at which an analog signal is measured and converted to digital data.
Serial port	A communication port for transferring data on a single line (bit serial). Other lines are often used for ground and initiating communication.
Signal-to-noise ratio (SNR)	The ratio of an rms sinusoidal input signal to the rms noise, usually expressed in deciBels.

T

Terminator (memory)	A resistive termination on the memory access bus to prevent signal reflections. Without termination, the reflections could cause erroneous data storage or readouts.
Throughput	The effective rate of data transmission through the waveform acquisition system. The sample rate, active memory length, data transfer rate to the host computer, host computer display or storage time, digitizer re-arm time, and time until trigger all reduce the waveform throughput time.
Time base	The sample period or time between two samples. This definition differs from that for an oscilloscope (time/CRT division), since either the entire 8828D digitized waveform or a waveform subsection can be displayed.
Trigger level	The adjustable voltage level which causes a trigger signal to be generated. For external (front panel input) trigger, this level can be adjusted via a front-panel potentiometer from -2V to +2V. A DC voltmeter connected to the front panel "Stop Trigger Threshold Test Point" will indicate the trigger level.
Trigger threshold	See Trigger level.

U

Unipolar signal — A dynamic signal which either contains only positive voltage levels or contains only negative voltage levels.

V

Vertical resolution — The total number of voltage levels (i.e., 256 for the 8-bit 8828D digitizer) or digital output code "counts". The vertical resolution is specified in terms of digital output bits for high speed "flash" type ADCs, such as used in the 8828D digitizer. For the 8828D, the vertical resolution is 8 bits which represents 4096 distinct levels.

Vertical sensitivity — The vertical resolution divided by the full scale voltage on the selected range. Determines the smallest detectable level on a single-shot acquisition. Signal averaging on repetitive signals can reduce the vertical sensitivity for a given full scale voltage range.

APPENDIX B: Description of CAMAC

CAMAC modules may be plugged into a CAMAC mainframe (called Crate in the CAMAC standard) which has up to 25 stations numbered 1 through 25. A station is a slot which accepts a CAMAC module. Some modules occupy several stations. The rightmost two stations are reserved for a Crate Interface or Controller whereas the remainder are Normal Stations used for instrumentation modules. The purpose of the crate controller is to issue CAMAC commands to the modules and transfer information between a computer and the CAMAC modules. It is the interface between the CAMAC Dataway and a computer.

All CAMAC operations take place over the CAMAC Dataway. The Dataway is a parallel bus used to transfer all data, the function coding information, and all status information. In a typical Dataway operation, the crate controller issues a CAMAC command which includes specifying a station number (N), a subaddress (A), and function code (F). In response, the module will generate a valid command accepted (X response) and act on the command. If this command requires data transfer, the read (R) or write (W) lines will be used. Note that the terms Read and Write apply to the crate controller, not the module. For example, under a read command, the crate controller reads data contained within a module.

Whenever there is no Dataway operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention.

There are also three common control signals made available at all stations:(Z) to Initialize all units, (C) to clear data registers, and (I) to Inhibit (e.g., data-taking).

Definition of CAMAC Commands

The CAMAC command consists of signals on the Dataway lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines, and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the Dataway.

Station Number

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station.

Subaddress Codes

Different sections of a module are addressed by signals on four A bus lines. These signals are decoded in the module to select one of up to 16 subaddresses, numbered in decimal from A(0) to A(15).

Function Codes

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines (F16, F8, F4, F2, F1). These signals are decided in the module to select one of up to 32 functions, numbered in decimal from F(0) to F(31). To see to which functions a particular LeCroy instrument reacts, see its manual.

CAMAC Data

A common parallel highway is used for all data transfers. All information carried by the parallel highway is conveniently described as data, although it may be information concerned with status or control features in modules. Up to 24 bits may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

The Write Lines

The crate controller generates data signals on the 24 parallel W bus lines (W1-W24) at the beginning of any Write operation.

The Read Lines

Data signals are set up on the 24 parallel R bus lines (R1-R24) by the instrumentation module as soon as a Read command is recognized. An interface such as the 8901A strobes data from the R bus lines into its own internal registers, whereafter the data is appropriately formatted for GPIB compatible transfers.

Status Information

CAMAC status information is conveyed by signals on the LAM, Busy (B), Response (Q) and Command Accepted (X) lines. This status information is similar to the GPIB service request.

Look-at-Me (LAM)

This, like the N Line, is an individual connection from each station to a separate pin at the control station. When there is no Dataway operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention, such as is the case when a waveform recorder has finished a conversion sequence. A LAM request can be reset by Clear LAM, Initialize, or by the performance of the specific action which generated the request. The CAMAC controller converts the LAM line into an IEEE-488 Service Request (SRQ).

Q Response

The Q busline is used during a Dataway operation to transmit a signal indicating the status of a selected feature of the module, such as whether or not data being read is valid.

Command Accepted

Whenever a module is addressed during a command operation, it must generate an X = 1 on the Command Accepted busline (X) if it recognizes the command as one that it is equipped to perform.

Command Controls and Signals

The following common control signals operate on all modules within the crate, without requiring address by a command.

Initialize

The initialize signal (Z) has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, and by resetting all LAM signals and disabling them where possible.

Inhibit

The presence of this signal (I) can be used by a module to inhibit any activity (for example, data-taking).

Clear

The common clear signal (C) resets all registers and bistables connected to it.

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